A Gallium Nitride Switched-Capacitor Power Inverter for Photovoltaic Applications

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***Abstract*—A Gallium Nitride (GaN) based switched-capacitor module integrated inverter (MII) is presented in this paper. This two stage solution first employs a dc/dc quadrupler that utilizes an interleaving charging scheme. This strategy not only reduces the high frequency current ripple subjected to the photovoltaic panel, but also decreases the voltage ripple on the DC link between the two stages. The second stage is a five-level boost inverter that is responsible for both maximum power point tracking (MPPT) and minimizing reactive power flow. Both stages utilize a resonant soft-switching scheme in the capacitor charging current loops to increase the MII's efficiency. Basic theoretical analysis and experimental results for the individual stages are included.**

I. INTRODUCTION

The United States (US), through its Department of Energy (DoE), is funding research to reduce the cost of photovoltaic (PV) power production to $1/W [1], [2]. Lowering the cost of the associated power electronics from $0.22/W to $0.1/W is part of this aim [1], [2]. With regards to residential power generation, the module integrated inverter (MII) is a topic of active research [2]-[7]. This approach offers several advantages over the conventional approach of using multiple panels with a single power conversion unit. Most importantly, the MII can harvest more energy from an array of panels because each panel in the array operates at its own maximum power point (MPP) [3]. Additionally, total system costs are reduced due to lower manufacturing costs that result from mass production and limited use of expensive DC components; such as fuses, and also by leveraging existing AC installation expertise [4]. Reliability is also improved since failures are typically isolated to a single device and power can continue to be supplied to the grid.

Researchers are already exploring the properties of emerging wide bandgap devices, specifically faster switching speeds, higher operating junction temperatures, and lower on-resistances [8]-[10], to see if they offer a competitive advantage over hardware created with silicon devices [5],[6]. Gallium Nitride demonstrations have included an interleaved boost converter for use in a Module Integrated Converter (MIC) [5], and a MII platform constructed of Z-source inverters [6]. In addition, [7] explores the possibility of eliminating bulky magnetic components through the application of a switched-capacitor based MIC.

This paper presents a two-stage Gallium Nitride (GaN) based switched-capacitor (SC) (Fig. 1) MII. The topology cascades a voltage quadrupling dc/dc converter with a five level inverter. The inverter performs maximum power point tracking (MPPT) while minimizing the reactive power flow. The quadrupler interleaves the charging current to reduce the current ripple [11] subjected to the PV panel. Switching losses are reduced by utilizing the LC resonance that exists between the energy storage capacitance and the printed circuit board's (PCB) stray inductance [12].

The proposed MII will serve as a prototype for a topology that is intended for future GaN based integrated circuits (IC). As [13] has already developed a 20 W three-phase inverter IC made from GaN, achieving this level of integration should be plausible in the near future.

The rest of the paper is structured as follows: section II presents a system level overview and discusses the individual cell structures that are used to build each stage. Section III provides a detailed analysis of the quadrupler. The five-level boost inverter is discussed in Section IV, and the paper concludes with experimental results for the quadrupler, and preliminary test results for both the inverter, and the proposed MII topology.

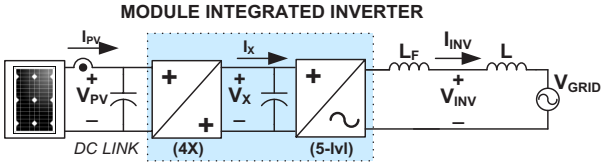


Figure 1. System diagram of module integrated inverter

II. SYSTEM OVERVIEW

A. System Overview

The proposed MII is designed for integration into a commercial PV panel that would be deployed in a typical 120 V_{RMS} residential system. These panels have a nominal MPP voltage (V_{MPP}) of 30 V (for an irradiance of 800 W/m^2) [14],[15]. A two-stage approach is employed where the first stage quadruples the PV voltage to a nominal 120 VDC, and the second stage (a five level boost inverter) generates a single phase sinusoidal output.

Each stage is built from one type of switched-capacitor cell [16]. The quadrupler is created from cascading the output of three isolation cells (Fig 2a) [17] with the input source. The five-level boost inverter is composed of two Marx cells (Fig 2b) [18] and four additional bypass switches. Using the PCB's stray inductance to achieve soft-switching has been demonstrated previously [12], [16], [19], and is applicable here for both cells. A series RLC circuit is used to model a single charging cycle, where R is the resistance (R_{DS_ON} and R_{ESR}) in the charging loop, L is the PCB's stray inductance, and C is the energy storage capacitance. This second order system has a characteristic equation given by

$$\frac{d^2 i(t)}{dt^2} + \frac{R}{L}\frac{di(t)}{dt} + \frac{1}{LC} i(t) = 0 \cdot \quad (1)$$

Assuming the system is severely underdamped, the current will approximate a sinusoidal waveform with a frequency of

$$f_s \approx \frac{1}{2\pi\sqrt{LC}} \cdot \quad (2)$$

Zero Current Switching (ZCS) is then achieved by setting the switch's on time to be

$$t_{on} = \frac{1}{2 f_s} \cdot \quad (3)$$

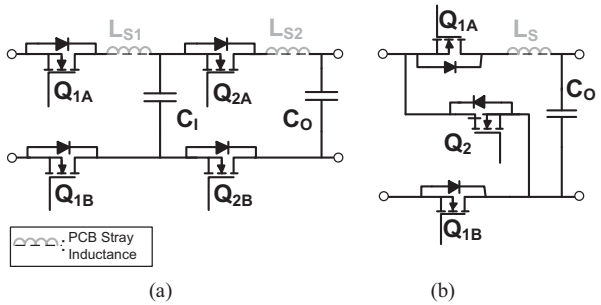
The advantages of the proposed circuit include:

1) Simple control

Though the system has a complex circuit structure, the modular design enables a simplistic control strategy. The quadrupler requires three control signals while the inverter needs only four control signals.

2) High boost ratio

The circuit realizes a high boost ratio without using any discrete inductive components.



(a) (b)

Figure 2. Schematics for the (a) isolation cell and the (b) Marx cell.

3) High efficiency with ZCS

Zero current switching can be realized in both the dc/dc and dc/ac stage to enable high efficiency

The main drawback or the challenge that still needs to be addressed is the high capacitance dc link required to filter the 120 Hz ripple, which is inherent to single phase circuits.

B. Cell Structures

An isolation cell is composed of four switches and two capacitors. It has two operating states. During the first half of operation, switches S_{1A} and S_{1B} are turned on, and energy is transferred to the intermediate capacitor (C_I). In the second half, S_{2A} and S_{2B} are turned on, and energy is transfer to the output capacitor (C_O) and the load. Since only two switches are conducting at a time, the output capacitor is isolated from the input source through a pair of switches [17]. With the aid of the stray inductance, both pairs of switches turn off under ZCS.

A resonant Marx cell is created from three switches and a single capacitor. Due to the manner in which this structure is implemented, each switch operates under a different type of stress [16], [19]. Because of the LC resonance between the cell's capacitor and the stray inductance in the circuit, one switch (Q_{1A} or Q_{1B} depending on the cell's orientation) can be turned off at zero current switching. For the other switch, either Q_{1B} or $Q_{1A,}$ the free-wheeling current enables it to turn off under zero voltage switching. However, the middle switch will always be hard-switched.

III. VOLTAGE QUADRUPLER

A. Operating Principles

The quadrupler achieves voltage multiplication by cascading the outputs of three isolation SC cells in series with the input voltage source (Fig. 3). In this particular topology, the input source (C_6) is connected between cells two (C_4) and three (C_8). Therefore, the voltage stress on the switches in cell one is $2V_{in}$ while switches in cells two and three are only subjected to V_{in}. To accommodate the source being inserted at this point, the switches in block three are reversed (i.e. the drain of S_9 and S_{10} are connected to the input). This prevents the source from being short circuited through the body diodes of S_9 and S_{11}.

The same structure can be realized with four isolation cells, however there are two advantages of using the input source in lieu of the additional block. First, though the total device power rating remains the same, the circuit has a reduced number of auxiliary circuits and control signals. Second, with a smaller number of components, additional losses are eliminated, and a greater efficiency is achieved since ¼ of the energy is directly supplied to the load from the source rather than being processed by additional circuitry.

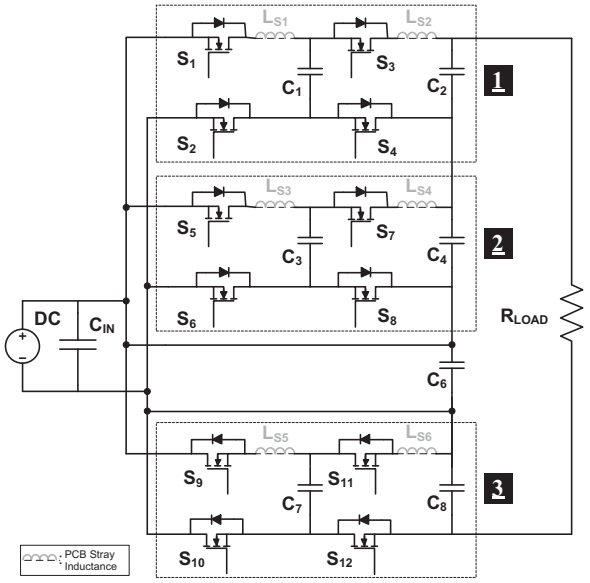


Figure 3. Schematic of the voltage quadrupler.

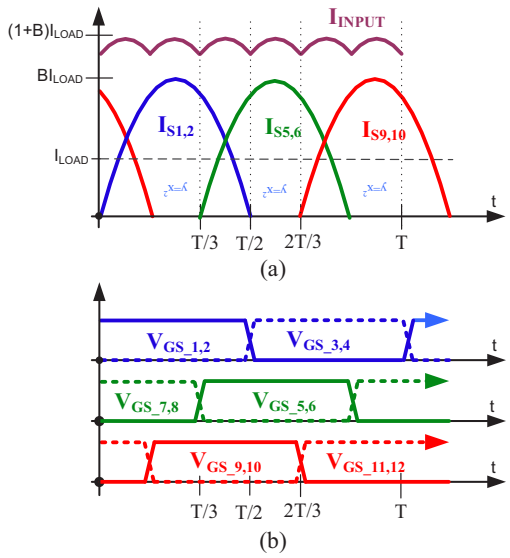


Figure 4. (a) Interleaving charging current and input current (b) along with associated control signals

Even with soft switching, pulsating charging current in switched-capacitor circuits can still result in significant power loss across the R_{ESR} on both the filter and storage capacitors. The solution is to use an interleaving charging strategy (Fig. 4a). The charging of each cell is phase-shifted by 120° to achieve this result (Fig. 4b). Thus, the high frequency ripple in the input current has been greatly reduced. In addition, the output capacitors are also charged a 120° out of phase from each other. By interleaving the voltage ripple on each of the capacitors, the overall voltage ripple seen by the load is reduced. Aside from decreasing the size of the DC link capacitors and minimizing the associated losses on the input capacitor and the dc bus capacitor, interleaving is necessary to realize MPPT by limiting the ripple that is exposed to the PV. The reduced fluctuation in the inverter's input voltage also improves the stability of the control system.

B. *Efficiency Analysis*

Three types of losses occur in this circuit; conduction, switching, and control losses. The conduction losses will result both from the load current and the charging current. Switching losses include those that are caused from I_D/V_{DS} rise and fall times as well as energy consumed through charging and discharging the output capacitance of the device. Control losses account for the charge supplied to the gate when the device turns on, as well as the energy that is consumed in the peripherals that operate the circuit.

1) *Conduction Losses*

The conduction losses in the quadrupler are broken into two parts; one associated with charging the intermediate capacitor in the first stage, and the other that results from providing energy to the output capacitance and the load. Since the output capacitance and stray inductance are, ideally, identical from cell to cell, the oscillation frequency of the first stage is lower than that of the second stage. This occurs because the intermediate capacitance is in series with the output capacitance during operation in the second stage, and the overall capacitance in the LC resonant loop is decreased.

In the output stage, when switches S_3 and S_4 are turn on, the following relationship can be derived (note: cell one is used for this analysis):

$$\frac{i_{C2}(t)+i_{S3}(t)}{C} = L\frac{d^2 i_{S3}(t)}{dt^2}, \tag{4}$$

from nodal analysis:

$$\frac{d\left(V_{C1}(t)-V_{C2}(t)\right)}{dt} = \frac{d\left(V_L\right)}{dt}. \tag{5}$$

If the change in the load current is assumed to be zero, then

$$\frac{d^2 i_{S3}(t)}{dt^2} \approx \frac{d^2 i_{C2}(t)}{dt^2}, \tag{6}$$

and the two currents can be written as

$$i_{C2}(t)+i_{S3}(t) = \frac{1}{2}LC\frac{d^2\left(i_{S3}(t)+i_{C2}(t)\right)}{dt^2}. \tag{7}$$

The result is that both currents are sinusoidal and each can be written as

$$i_{S3}(t) = A\sin(w_2 t+\varphi)+\frac{I_{LOAD}}{2}, \text{ and} \tag{8}$$

$$i_{C2}(t) = A\sin(w_2 t+\varphi)-\frac{I_{LOAD}}{2}, \tag{9}$$

where ω_2 is equal to $\sqrt{2}/\sqrt{L_{S2}C_T}$ and C_T is the series combination of C_1 and C_2. Through the principle of conversation of charge, it is determined that A = 3.1275 I_{LOAD} and φ = - 9.20°. These values are only valid when the stray inductances and the capacitances are identical from stage to

stage. Furthermore, the duty cycles will be D_1=0.562 and D_3 =0.438. The power loss can then be calculated as

$$P_{CON,S3} = \frac{1}{2\pi}\int_0^{0.876\pi}\left(A\sin(\frac{\theta}{0.744}+\varphi)+\frac{I_{LOAD}}{2}\right)^2 R_{DS\_ON}d\theta \text{, and}$$
$$= 2.66 I_{LOAD}{}^2 R_{DS\_ON} \quad (10)$$

$$P_{CON,C2} = \frac{1}{2\pi}\int_0^{0.876\pi}\left(A\sin(\frac{\theta}{0.744}+\varphi)-\frac{I_{LOAD}}{2}\right)^2 R_{ESR}d\theta \quad (11)$$
$$= 1.25 I_{LOAD}{}^2 R_{ESR}$$

respectively.

In the intermediate stage, the charging current through both the capacitor and the switches are the same, and can be approximated as

$$i_{S1}(t) = i_{C1}(t) = B\sin(w_1 t)\,. \quad (12)$$

The constant *B* can be determine through again applying conservation of charge

$$\int_0^{1.124\pi} B\sin(\frac{\theta}{1.124})d\theta = 2\pi I_{LOAD}\,, \quad (13)$$
$$B = 2.195 I_{LOAD}$$

and the power loss can be estimated as

$$P_{CON,S1+C1} = \frac{1}{2\pi}\int_0^{1.124\pi}\left(B\sin(\frac{\theta}{1.124})\right)^2 (R_{DS\_ON}+R_{ESR})d\theta \,. \quad (14)$$
$$= 2.195 I_{LOAD}{}^2\left(R_{DS\_ON}+R_{ESR}\right)$$

2) Switching Losses

A carefully designed quadrupler will transition under ZSC conditions. Therefore, the corresponding losses will effectively be zero. However, the energy transferred to the output capacitance during each switching transition will still be consumed. It is accounted for by recognizing that

$$P_{SW,Sx} = \frac{1}{2} C_{OSS} V_{DS}{}^2 f_s\,. \quad (15)$$

3) Control Losses

The control losses are difficult to estimate without a detailed design. It includes the power consumed by all the auxiliary logic that is used to not only drive the circuit, but also any other hardware that is responsible for safe guarding the implementation. However, the amount of power required by the gate driver to turn the switch on and off can be determined by

$$P_{GD,Sx} = Q_G V_{GS} f_s\,. \quad (16)$$

4) Estimated Losses

Table I lists the parameters used in the design of the quadrupler. These values were used to estimate the multiplier's efficiency under normal operating conditions. For the results provided in Table II, (14) has been broken up into two parts, one for the switch and another for the intermediate capacitor. The R_{ESR} calculated in Table I is for a single 1 μF capacitor. This value is divided by four in the estimates below because the actual circuit uses four capacitors in parallel. The different calculations for the output capacitor loss account for cell one blocking *2 V_{in}* and cells two and three blocking *V_{in}*.

TABLE I. ESTIMATION PARAMERTERS

Paramater	Value
V_{in}	30 V
V_{GS}	5 V
f_S	350 kHz
R_{DS_ON}[a]	25 mΩ
R_{ESR}[b]	22.7 mΩ
C_{OSS}[a]	400 pF
Q_G[a]	7.5 nC

a – EPC-1010 GaN HEMT [20]
b- TDK C5750X7R2E105K [21]

IV. FIVE-LEVEL INVERTER

A multilevel switched-capacitor (SC) inverter with boost function was selected for this application. The five-level SC inverter, as shown in Fig. 5, is created by placing the input source in the middle of two Marx cells. Four additional bypass switches are required to shift the output voltage from $|V_{out}| = V_{in}$ to $|V_{out}| = 2V_{in}$. A multicarrier PWM strategy is used to modulate between different switching states. This is accomplished by breaking a fundamental cycle up into six regions (Fig. 6), each of which have two switching vectors (Table III) associated with them. To minimize the inverter's switching losses; a maximum of three switches change states

TABLE II. ESTIMATED POWER LOSS OF QUADRUPLER

Output Power	Output Current	Estimated Loss for the Circuit										Gate Drive Loss	
		Conduction Loss (W)				Output Cap. Cell 1 (W/sw.)	Output Cap. Cell 2 &3 (W/sw.)	Total Loss (W)			Eff (%)	Single Device (mW)	Circuit (mW)
		S_1	C_1	S_3	C_2			Cell 1	Cell 2&3	Circuit			
50 W	0.417 A	0.01	0.002	0.012	0.005	0.252	0.063	1.057	0.301	1.660	96.7%	13.1	157.5
100 W	0.833 A	0.038	0.009	0.046	0.02	0.252	0.063	1.205	0.449	2.103	97.9%	13.1	157.5
150 W	1.25 A	0.086	0.019	0.104	0.044	0.252	0.063	1.451	0.695	2.841	98.1%	13.1	157.5
200 W	1.667 A	0.152	0.035	0.185	0.079	0.252	0.063	1.796	1.04	3.875	98.1%	13.1	157.5
250 W	2.083 A	0.238	0.054	0.289	0.123	0.252	0.063	2.239	1.483	5.204	97.9%	13.1	157.5
300 W	2.5 A	0.343	0.078	0.416	0.177	0.252	0.063	2.780	2.024	6.829	97.7%	13.1	157.5

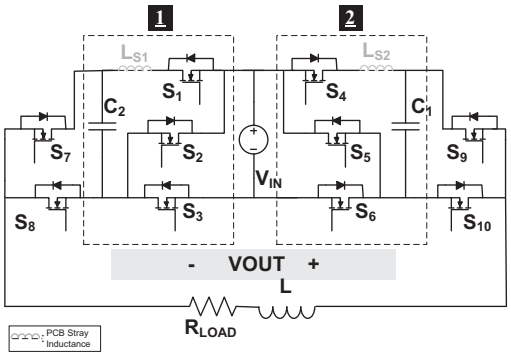


Figure 5. Five-level switched-capacitor inverter.

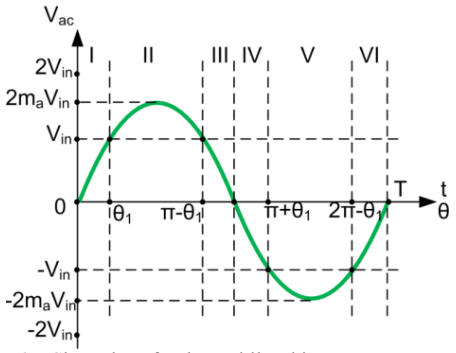


Figure 6. Six regions for the multilevel inverter PWM strategy.

TABLE III. SWITCHING VECTOR FOR MULTI-LEVEL INVERTER

Vector	*Switching vectors of the five-level switched-capacitor inverter*									
	Output Voltage	$S_{1,3}$	S_2	$S_{4,6}$	S_5	S_7	S_8	S_9	S_{10}	*Section*
V1	2Vin	1	0	0	1	0	1	1	0	II
V2	Vin	1	0	0	1	0	1	0	1	
V3	Vin	1	0	0	1	0	1	0	1	I, III
V4	0	1	0	1	0	0	1	0	1	I, III, IV, VI
V5	-Vin	0	1	1	0	0	1	0	1	IV, VI
V6	-Vin	0	1	1	0	0	1	0	1	V
V7	2Vin	0	1	1	0	1	0	0	1	

when transitioning between any two adjacent vectors.

Soft switching is accomplished by fixing the charging time, $T_{CHG,}$ for $S_{1,3}$ and $S_{4,6}$ to the time interval that achieves soft-switching. This requires the carrier frequency to change as the output transitions through the fundamental cycle. The relationship given by

$$T_{CHG}(t) = \left(1 - D(t)\right)\frac{1}{f_{SW}(t)}, \tag{17}$$

where D(t) is the on time of S_2 and S_5 at each particular instance of the fundament cycle and can be calculated from

$$D(t) = \begin{cases} 2m_a \sin(\omega t) - 1, & \theta_1 < \omega t < \pi - \theta_1 \\ -2m_a \sin(\omega t) - 1, & \pi + \theta_1 < \omega t < 2\pi - \theta_1 \end{cases}. \tag{18}$$

To simplify the implementation, the carrier frequency is only modulated during regions II and V. In the other four regions, the inverter functions as an H-bridge. One caveat about this method is that the fixed charging interval and the maximum switching speed of the device constraints the upper limit of the modulation index. This was one of the motivating factors for using the quadrupler to provide the required headroom.

V. EXPERIMENTAL RESULTS

A. Test Setup

The quadrupler and the inverter are constructed from a universal GaN based switched-capacitor test module (Fig. 7) [19]. Each module can accommodate up to six EPC-1010 [20] devices. The boards are laid out so that the user can configure each module as either an isolation cell, or a cascade of two Marx cells.

Power for each test setup is provided by a DC source. A resistor bank is used to load the device under test, and control is provided by a Texas Instruments DSP microcontroller (TMS320F2812). Efficiency measurements are made using a Yokogawa WT3000 in conjunction with LEM Danfysik IT 700-S current transducers.

B. Quadrupler Testing

Three GaN test modules are required to create the quadrupler. Each isolation cells is constructed with the intermediate and output capacitance created from four 1 µF capacitors in parallel. Soft-switching is realized using a switching frequency of 350 kHz and a duty ratio of 0.45 for the first stage. Using (3), the stray inductance is estimated at 39.5 nH.

Efficiency testing was performed at the rated operating conditions with a 30 V source at the input. A 10 µF film capacitor is connected to the output of the quadrupler to filter

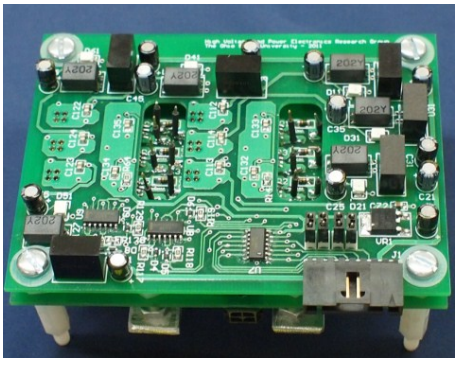


Figure 7. Universal Gallium Nitride switched-capacitor module.

out the high frequency ripple. A peak efficiency (Fig. 8) of 95.4 % was obtained at a load of 150 W.

The operating waveforms for the 300 W test are shown in Fig. 9. It can be seen that switches $S_1$and S_2 as well as S_5 and S_6 turn off as the charging currents, I_{C1} and I_{C3}, reach zero, thereby realizing ZCS. Also shown is the interleaving operation of the two charging currents for cells one and two. The two waveforms are not entirely symmetrical due to the fact the test setup was created from an interconnection of modules. The variation in the cables between the modules, results in values for the inductances, L_{S1}, L_{S3}, and L_{S5} that are slightly different from each other. Furthermore, this wiring adds additional resistance, which is significant due to the skin effect. It is also a reason for the efficiency numbers being lower than predicted values. Results can be greatly improved if the topology is integrated onto a single PCB.

C. *Five-Level Inverter Testing*

Two universal modules are used to construct the five-level inverter. The output capacitor is composed of three 1 µF capacitors connected in parallel. Several low voltage tests have been conducted on the inverter, and a peak efficiency of 97.3% was obtained for an output of 100 W with a 40 V input.

An entire fundamental cycle is displayed in Fig 10. I_{C2} is the charging current being supplied to C_2 from switches S_4 and S_6. Figure 11 shows the inverter achieving soft switching at the peak charging current (the red circle in Fig. 10).

D. *System Testing*

The MII is still under evaluation, so the results are limited to low voltage and low power testing. The preliminary tests performed on the MII test setup are shown in Fig. 12. The quadrupler's input voltage was fixed to 7.5 V while the MII outputs 30 W. During the test, to cope with the 120 Hz ripple, a 2 mF capacitor is added to the output stage of the quadrupler.

CONCLUSIONS

A two stage Gallium Nitride, switched-capacitor based module integrated inverter has been presented. Experimental results verify the quadrupler is capable of operating at rated power while still being able to achieve soft switching. Also shown, is a five-level inverter that is capable of achieving soft-switching through modulating the carrier frequency. Finally, preliminary experimental results for the module integrated inverter demonstrate the systems operation at low power.

Future work includes 1) pushing the MII input voltage to 40 V and the input power to 300 W; 2) performing theoretical analysis on optimized cell capacitance and control strategies to reduce the total capacitance requirement for the 120 Hz current ripple.

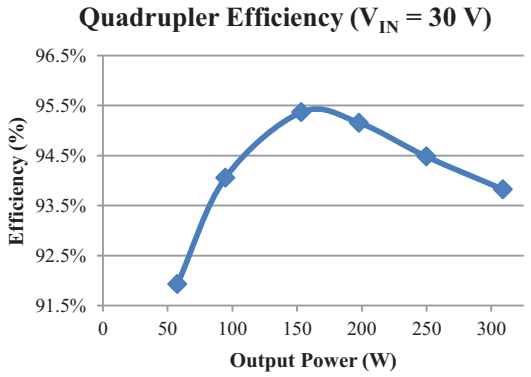


Figure 8. Quadrupler efficiency results.

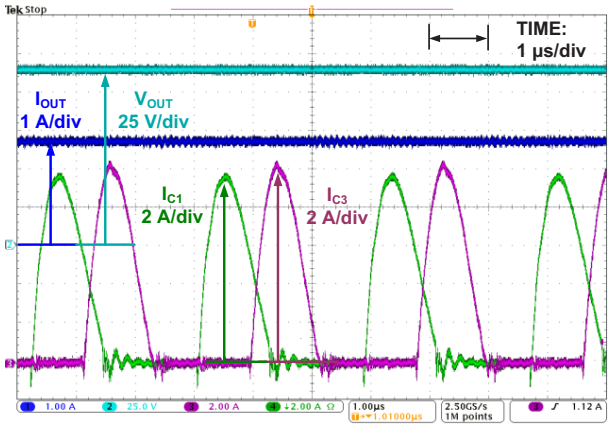


Figure 9. Quadrupler charging current and output waveforms (V_{IN}-30 V, P_{OUT} = 300 W).

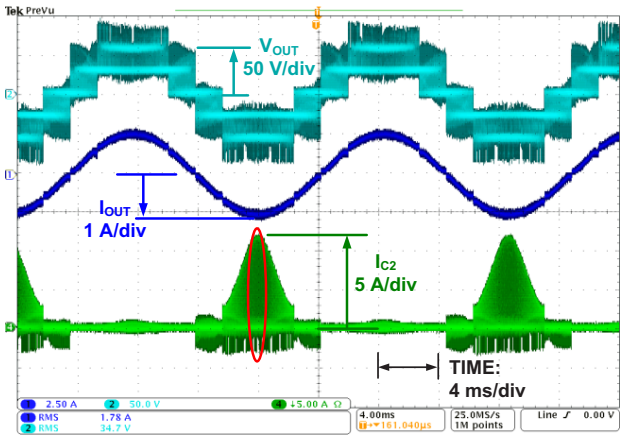


Figure 10. Five-level inverter output waveforms and charging current.

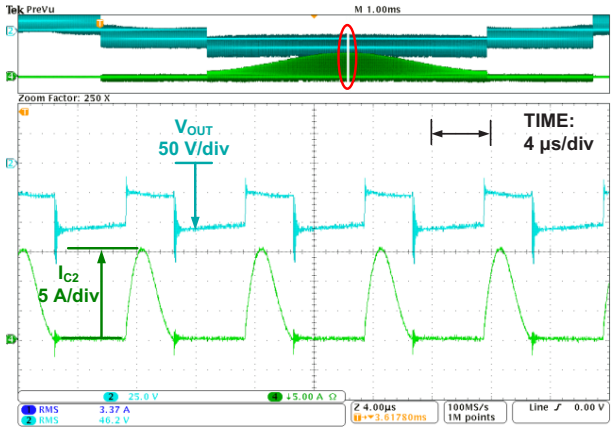


Figure 11. Five-level inverter charging current and output voltage.

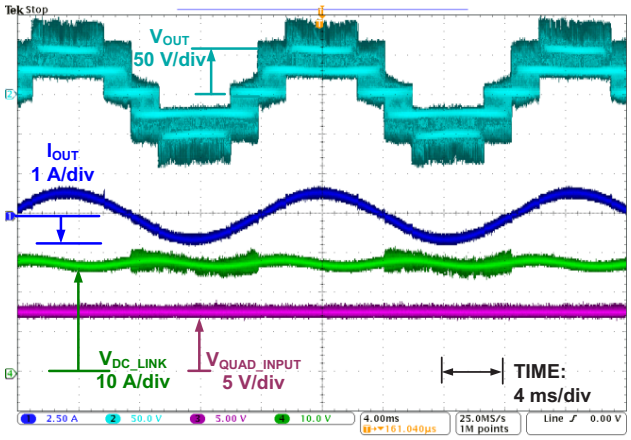


Figure 12. MII input voltage, dc-link voltage, and output waveforms.

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