A Switched-Capacitor Voltage Tripler With Automatic Interleaving Capability

Ke Zou, *Student Member, IEEE*, Mark J. Scott, *Student Member, IEEE*, and Jin Wang, *Member, IEEE*

***Abstract*—This paper presents a high-efficiency switched-capacitor voltage tripler topology aimed at high-power applications. A soft-switching scheme without the addition of extra components is adopted to minimize the switching loss and the electromagnetic interference noises. A two-step current charging method is used to enable the input current and output voltage interleaving functionality without adding an excessive number of components. The large loss on the input capacitor that exists in the traditional switched-capacitor topologies is eliminated by employing this interleaving scheme. The soft switching and interleaving results are analyzed in detail. The experimental results for a 2-kW prototype are demonstrated to verify the functionality of the proposed topology.**

***Index Terms*—Interleaving operation, soft switching, switched-capacitor circuits.**

I. Introduction

THE switched-capacitor circuit concept has been widely adopted in small-scale power conversions. By eliminating the inductive components in the circuit, switched-capacitor converters possess the advantages of light weight, low volume, and high power density. Various topologies and control methods have been proposed and successfully applied [1]–[6].

However, the traditional switched-capacitor converter topology and associated analyzing methods have significant drawbacks that hamper their application in higher power level conversions where high efficiency and low components stress are emphasized. On the topology side, many classical circuit topologies, such as the traditional charge pump circuit, place large voltage stresses on the capacitors, or require huge input or output capacitors. On the control side, capacitor charging current is traditionally not controlled, which subjects the semiconductor switches to large current stress, reduces the efficiency of the converter, and generates a large amount of electromagnetic interference. Moreover, since the existing methods of regulating the output voltage can lower the efficiency, they are not feasible for large-scale switched-capacitor converters.

Several novel topologies and control methods have been developed in recent years to solve the aforementioned problems and push the switched-capacitor converter to higher power levels. A switched-capacitor dc–dc converter based on the generalized multilevel converter topology is presented in [7]. It can realize bidirectional power conversion between a 42-V battery and 14- or 42-V loads. However, it requires a large number of switches and capacitors. In [8], a 3X (i.e., the output voltage is three times the input voltage) dc–dc multiplier/divider was proposed and a 55-kW prototype was built. However, in this topology, the duty ratio for the capacitor charging time is only 1/3, which results in a higher peak charging current, and thus reduces the efficiency. In [9], a multilevel modular capacitor-clamped dc–dc converter topology (MMCCC) was proposed with many benefits, including its modular structure, lower current and voltage stress placed on the switches, and bidirectional operation capability. A detailed analytical approach to calculate the capacitor and load voltage of MMCCC is presented in [10]. Nevertheless, it still has several problems when used in high power applications, including a large number of capacitors and high input current ripple. The input current ripple leads to significant conduction losses on the input capacitor and may affect the lifespan of the input power source. To solve the large input current ripple problem of the MMCCC topology, an interleaving structure is presented in [11]. Another switched-capacitor converter using the interleaving method, but with a lower power rating, was published in [12]. A mixed control scheme is used in this paper to realize accurate interleaving. Although this traditional interleaving structure can effectively reduce the input current ripple, it requires a large number of components, which may increase both the converter cost and the chance of component failure. In [13], a switched-capacitor cell-based converter topology is introduced with multiple voltage output capability. It still has the problems of large input current ripple and small charging current duty ratio when the voltage conversion ratio is high.

Charging current regulation is an important part of improving the efficiency of switched-capacitor converters. Previous studies [14], [15] simplified this charging current by neglecting the stray inductance in the charging loop. These assumptions, although simple and effective in low-power switched-capacitor converters, may not be valid in higher power applications where the stray inductance in the current charging loop cannot be neglected. In [16]–[18], the quasi-resonant switched-capacitor converters are investigated where an extra inductor is added to form an oscillation loop with the capacitors to achieve soft switching. In [19], a switched-capacitor-based resonant converter using a phase-shift control method is proposed to realize the zero voltage switching. In [20], an improved soft-switching scheme, which does not require adding extra inductive

Manuscript received May 20, 2011; revised July 30, 2011 and October 3, 2011; accepted November 11, 2011. Date of current version March 16, 2012. This work was supported by the National Science Foundation (NSF) under project number 1054479. Recommended for publication by Associate Editor V. Agarwal.

The authors are with the Department of Electrical and Computer Engineering, Ohio State University, Columbus, OH 43210 USA (e-mail: zou.35@buckeyemail.osu.edu; scott.585@osu.edu; wang@ece.osu.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2011.2178102

components, is proposed. Since the charging current can be controlled using this soft-switching method, both the conduction loss and switching loss can be largely reduced.

For many large power applications, such as the front dc–dc converter in hybrid electric vehicles (HEVs), a large voltage conversion ratio is not needed and usually a voltage conversion ratio of three or four is sufficient. Moreover, for this dc–dc converter, efficiency, cost, and volume are more important than the accuracy of the output voltage regulation. Based on these observations, this paper presents a high-efficiency switched-capacitor voltage tripler that employs soft switching and current/voltage interleaving. The interleaving operation is automatically achieved without adding extra components. This paper introduces three different voltage triplers based on the proposed topology.

The rest of this paper is organized as follows: in Section II, a detailed analysis of the factors that affect the efficiency of a high-power switched-capacitor dc–dc converter is presented. Based on this analysis, Section III introduces the proposed voltage tripler topology and the associated two-step charging scheme. Functional analysis of the proposed converters, including soft switching, input current interleaving, and output voltage interleaving functions, is presented in Section IV. Finally, the experimental results for a 2-kW modular converter prototype are presented in Section V. Conclusions are presented in Section VI.

II. Methods to Minimize the Power Loss in a Switched-Capacitor DC–DC Converter

There are four types of power losses in a switched-capacitor converter: the capacitor charging loss, conduction loss, switching loss, and control circuit loss [21]. Since the capacitor charging loss and the control loss mainly depend on the capacitance of the capacitors or the switching frequency, only the other two types of losses, the switching loss and conduction loss, will be analyzed here.

A. Minimizing the Switching Loss—Soft Switching

A simple circuit to analyze the charging current of a switched-capacitor converter is the series *RLC* circuit shown in Fig. 1(a). In this circuit, the switch S is closed at $t = 0$. The voltage source ΔV represents the voltage difference between the voltage sources and the capacitor being charged. The stray inductance and resistance of this current charging loop are lumped together as L_S and R_S. For this *RLC* circuit, the charging current $i_{\rm ch}(t)$ can be expressed using the differential

$$\frac{d^2(i_{\rm ch}(t))}{dt^2} + 2\alpha\frac{di_{\rm ch}(t)}{dt} + \omega_0^2 i_{\rm ch}(t) = 0 \tag{1}$$

where $\alpha = R_s/2L_s$, the angular oscillation frequency $\omega_0 = 1/\sqrt{L_s C}$, and the damping factor is calculated as

$$\varsigma = \frac{\alpha}{\omega_0} = \frac{R_s}{2}\sqrt{\frac{C}{L_s}}. \tag{2}$$

The damping factor determines the shape of the charging current. Fig. 1(b) shows the shape of the charging current at three different damping factors in one switching cycle of a switched-capacitor converter. The switching frequency of this converter is 20 kHz. It can be seen in Fig. 1(b) that with a damping factor of 10, the charging current has only a small oscillation and can be regarded as a square waveform. While with a damping factor of 0.1, the shape of the charging current is almost sinusoidal. In this case, if the charging time is adjusted to be close to half the oscillation cycle of the series *RLC* circuit, the turn OFF transient of the switch S occurs at nearly zero charging current condition. As a result, zero current switching (ZCS) can be achieved.

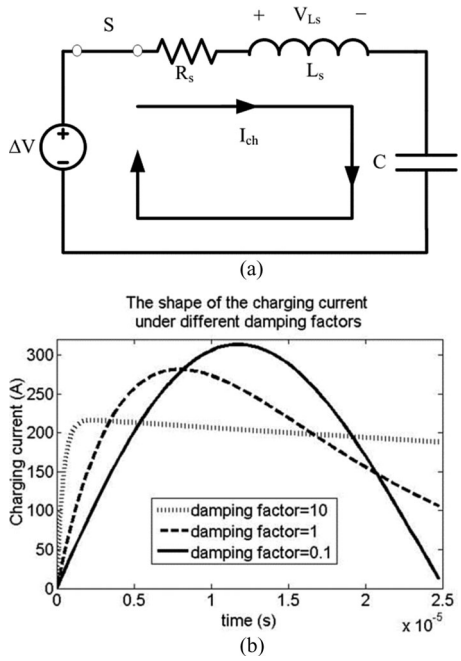

Fig. 1. (a) *RLC* equivalent circuit for the current charging loop. (b) Shapes of the charging current under different damping factors.

For converters with large current ratings, it is required that both capacitors have low equivalent series resistance (ESR) and the switches have low on-resistance to guarantee the high efficiency. The large physical size of the converter may also result in a large stray inductance of the charging loop. In this case, the loop resistance may not dominate in the charging current equation and the damping factor can be much smaller than 1, which will result in a sinusoidal charging current shape. The smaller the damping factor, the more sinusoidal the charging current shapes. For the purpose of simplicity, the following analysis assumes that the damping factor is much smaller than 1 and the charging current has a pure sinusoidal shape.

To realize this soft-switching scheme, it is important for the charging loop to have sufficient stray inductance so that the oscillation frequency is small enough to be achieved by available semiconductor devices. The adoption of devices with higher switching frequency will significantly reduce the requirement of both capacitance and stray inductance. Therefore, this soft-switching scheme can be easily realized by wide bandgap switching devices, which have high switching capabilities. With the assumption that the capacitance and stray inductance are reduced by the same proportion, and the loop resistance remains constant, the damping factor will not be affected.

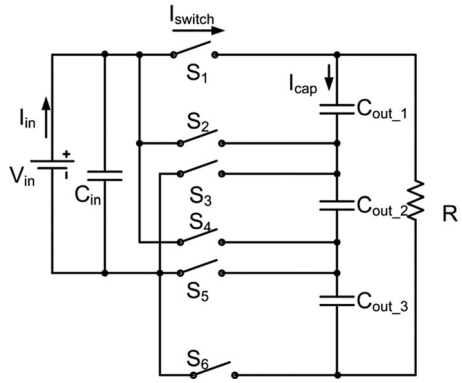

Fig. 2. 3X "direct charging" switched-capacitor dc–dc converter.

By implementing the soft-switching scheme, the switching power loss can be minimized, the large in-rush charging current can be avoided, and high efficiency can be achieved. The sinusoidal current shape is also a prerequisite for other control methods, such as the interleaving method, to improve the efficiency.

B. Minimizing the Conduction Loss—Reducing the Intermediate Stages

If soft switching is achieved, the converter losses mainly come from the conduction loss of the switching devices and the capacitors. There are mainly three types of capacitors in a switched-capacitor converter: input capacitors, output capacitors, and the intermediate capacitors. The input capacitors and output capacitors are connected to the input voltage source and the load, respectively. They are required in a dc–dc circuit to filter out the input and output voltage ripple. The intermediate capacitors are added to aid in the energy transfer from the input capacitors to the output capacitors.

The most effective way to reduce the conduction loss is to reduce the number of intermediate capacitor stages from the source to the load. A type of "direct charging" topology can be developed based on this principle. A 3X "direct charging" converter is shown in Fig. 2. In this converter, there are no intermediate capacitors. There is only one input capacitor and the output capacitor consists of three capacitors in series. The dc source charges each output capacitor in turn. Although the intermediate stages are eliminated in this converter, there are several flaws that hinder it from being used in high power applications. First, the voltage stress on each switch is large. In this 3X converter case, each switch either needs to block a voltage that is two times the input voltage or needs to block both positive and negative voltages with a value equal to the input voltage. This will dramatically increase the cost, conduction losses, and the difficulty of realizing soft switching. Second, this topology is based on a time-sharing charging principle, so the charging time allowed for each capacitor is 1/3 of a switching cycle. This will increase the peak charging current and reduce the efficiency. Furthermore, the input current ripple is large and a huge input capacitor bank is required, which also increases the cost and reduces the efficiency.

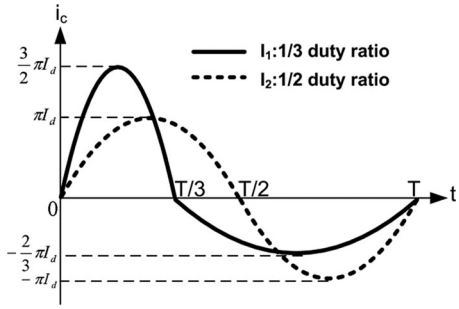

Fig. 3. Capacitor currents of two cases with different duty ratios in one switching cycle.

Due to the aforementioned direct charging topology problems, the next best candidate should be a topology with only one intermediate stage, which is the case with the proposed converter.

C. Minimizing the Conduction Loss—A 50% Duty Ratio for the Charging and Discharging Currents

For a converter with one or more intermediate capacitor stages, the conduction loss is determined by the shape of the charging and discharging currents. It is desired for the intermediate capacitors to continuously work at either charging or discharging such that there is no "idle" state. In this way, time is fully utilized and the peak charging current is smaller.

In one switching cycle, the intermediate capacitors need to be first charged and then discharged. The capacitor charging and discharging current during a switching cycle T of two different cases is shown in Fig. 3. The load current is assumed to be I_D in both cases, so the amount of electric charges that needs to be delivered to the load in one switching cycle is $T \times I_D$. The solid curve I_1 represents a sinusoidal capacitor current with a duty ratio of 1/3 for the charging part. In the last two-thirds of the cycle, the capacitor is discharging. The current I_2, represented by the dashed curve, is also sinusoidal, but with 0.5 duty ratio for the charging part.

The peaks of the charging part of the current I_1 can be calculated using

$$2D \times \int_0^{\pi} I_{1\_\mathrm{peak\_ch}} \times \sin(\theta) d\theta = I_D \times 2\pi. \tag{3}$$

Solving this equation, the peak of the charging part of I_1 is $3\pi/2 \times I_D$. Similarly, the peak of the discharging part of I_1 is $2\pi/3 \times I_D$. The peak of both the charging and discharging part of I_2 can be calculated to be $\pi \times I_D$.

Assuming R_S is the equivalent loop resistance, the conduction power loss of I_1 and I_2 can be calculated as in

$$P_{\mathrm{loss1\_ch}} = \frac{2}{3} \times \frac{1}{2\pi} \int_0^{\pi} \left(\frac{3\pi}{2} I_D \times \sin(\theta) \right)^2 R_S d\theta = \frac{3\pi^2}{8} I_D^2 R_S. \tag{4}$$

$$P_{\mathrm{loss1\_dis}} = \frac{4}{3} \times \frac{1}{2\pi} \int_0^{\pi} \left(\frac{2\pi}{3} I_D \times \sin(\theta) \right)^2 R_S d\theta = \frac{3\pi^2}{16} I_D^2 R_S. \tag{5}$$

$$P_{\text{loss1}} = P_{\text{loss1\_ch}} + P_{\text{loss1\_dis}} = \frac{9\pi^2}{16} I_D^2 R_S. \tag{6}$$

$$P_{\text{loss2}} = 2 \times \frac{1}{2\pi} \int_0^{\pi} (\pi I_D \times \sin(\theta))^2 R_S d\theta = \frac{\pi^2}{2} I_D^2 R_S \tag{7}$$

$$\frac{P_{\text{loss1}}}{P_{\text{loss2}}} = 112.5\%. \tag{8}$$

From the power loss comparison, it can be seen that a larger conduction power loss will be generated for the 1/3 duty ratio of the charging current compared to the 1/2 duty ratio.

The relationship between the duty ratio d and the power loss on the intermediate capacitor can be expressed in a form of

$$P_{\text{loss\_}c} = \left(\frac{1}{d} + \frac{1}{1-d}\right) \frac{\pi^2}{8} I_D^2 R_S \tag{9}$$

where d is the duty ratio of the charging current.

The optimized d, which minimizes the conduction loss, is 0.5. For most switched-capacitor topologies, the currents that go through the switches will be the same as either the charging or discharging currents of the intermediate capacitors. Therefore, the loss on the intermediate capacitors can represent the conduction loss of the switches in a switched-capacitor circuit. As a result, the conduction loss on the switches can also be minimized using 0.5 duty ratio charging current.

Another benefit of using the 50% duty ratio charging current is that the charging and discharging time of the capacitor is the same. Therefore, one single switching frequency can be adopted to realize soft switching on both the switches used to charge and those used to discharge the intermediate capacitors. This results in an easier circuit realization.

D. Losses on the Input Capacitor—The Interleaving Operation

The aforementioned loss analysis only considers the losses on the switches and intermediate capacitors. However, the large power loss occurring on the input capacitor should also be addressed. In fact, due to the sinusoidal charging/discharging current shape, the input capacitor suffers from large ac ripples. This requires a huge input capacitor to filter out the noise, but still any remaining noise may affect the lifespan of the power source.

An effective way to solve the large input current problem is to use the interleaving structure. The output capacitance can also be largely reduced by employing this interleaving scheme. The traditional interleaving concept uses several identical switched-capacitor converter modules in parallel with a constant phase shift between the modules. The main problem of this scheme is the large number of components that needs to be added. Although the current rating of each single device can be reduced using the interleaving structure, the voltage of each component remains the same, which can cause an increase in the cost and volume. A more serious problem is that by adding more components to the converter, the chance of component failure increases.

In order to eliminate the large input capacitor, increase the efficiency, and at the same time maintain low cost and high reliability, a topology that can realize the interleaving without adding extra components is needed.

III. Proposed Voltage Tripler With Interleaving Capability

A. Structure

As discussed previously, to achieve high efficiency, a desirable switched-capacitor topology should have the following features: ease of soft-switching realization, minimum intermediate capacitor stages, a 50% charging current duty ratio, and interleaving capability.

A 3X converter or voltage tripler based on this concept is shown in Fig. 4(a). In this converter, three stages with an identical structure, including two capacitors and four switches, are used. The output voltage is derived from the three stages stacked together. The structure of one single stage was first introduced in [22], with the purpose of separating the ground of the input and output voltages. This paper adopted this idea so that the input source can be isolated from the output capacitors and interleaving can be achieved without shorting two different voltage potentials.

For each stage, a two-step charging scheme is used. All the switches within one step are switched together while the switches in different steps work in complimentary mode. Take the top stage, for example, as shown in Fig. 4(b); S_1 and S_2 are switched ON in the first step while S_3 and S_4 are switched ON in the second step. Assume that the turn-ON duty ratio of the first step and second step are D_1 and D_2, respectively. Ideally, D_1 and D_2 should be both 0.5, and thus, the conduction loss can be minimized. The switching frequency is adjusted so that soft switching can be achieved on both steps. In reality, since a deadtime has to be added in the switching cycle, D_1 and D_2 cannot reach 0.5 simultaneously. To minimize the conduction loss, D_1 should equal D_2.

In the first step, the voltage source charges the intermediate capacitor C_1 through S_1 and S_2. At the same time, the output capacitor C_4 discharges to the load with a load current of I_D. If a 120° phase shift is applied among the three stages, input current interleaving can be achieved with maximum effect. The charging current of the first stage and the total input current under this interleaving operation are shown in the top and middle plot in Fig. 4(c), respectively. The three dotted waveforms in the middle plot are the charging currents of each stage while the solid waveform is the total input current.

In the second step, C_1 charges C_4 through S_3 and S_4 with a charging current of I_{C4}. At the same time, C_1 provides the load current I_D to the load, so the total current that goes through S_3 and S_4 equals the sum of I_D and I_{C4}. To achieve ZCS of S_3 and S_4, the charging current needs to have a sinusoidal shape but with an angle spanning more than half of a cycle. The current waveforms of the switch S_1 and the output capacitor C_4 are shown in the bottom plot of Fig. 4(c). With a 120° phase shift between each two stages, the output voltage ripple can also be largely reduced. The details of the interleaving effect will be studied in Section IV.

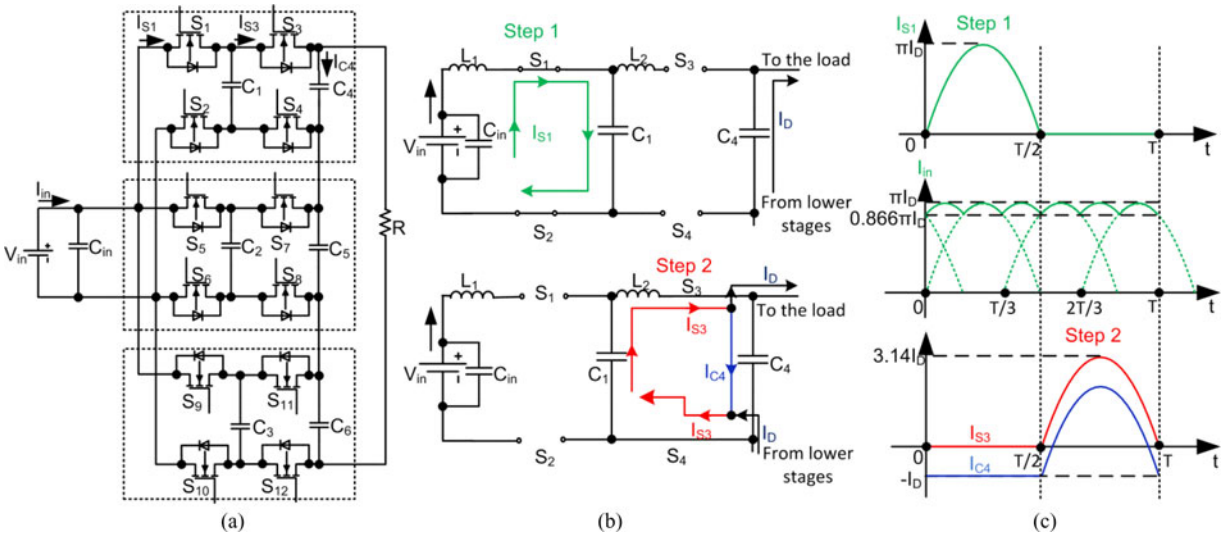

Fig. 4. (a) Structure of the proposed 3X converter. (b) Two switching steps in the top stage. (c) Current waveforms of the top stage.

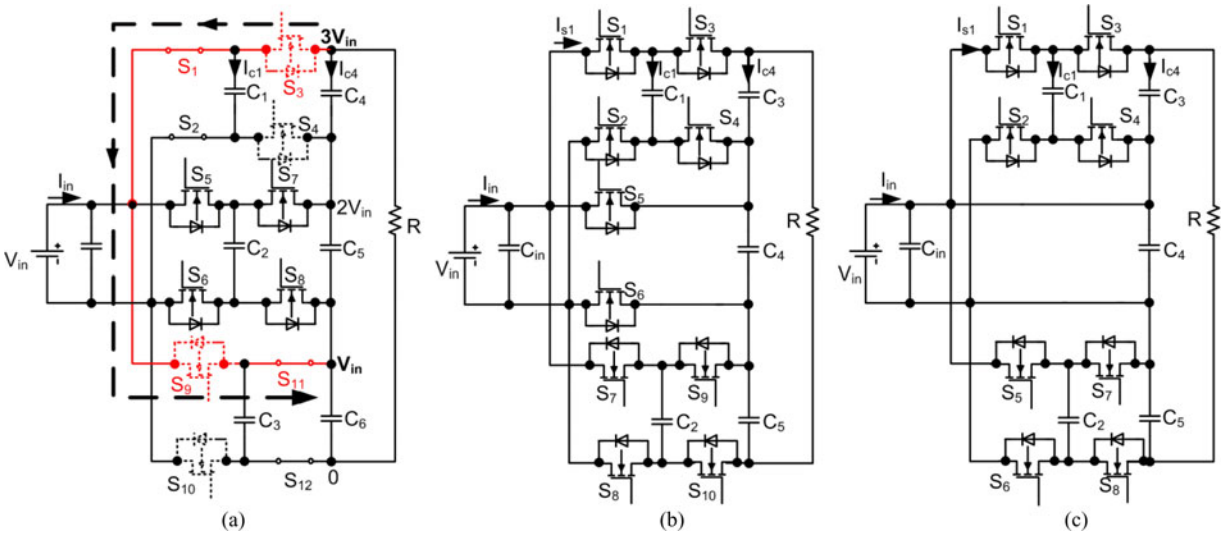

Fig. 5. (a) One operation state showing a path with two OFF-state switches. (b) 3X converter with only two switches in the middle stage. (c) 3X converter with no component in the middle stage.

B. Component Stress Analysis

All the capacitors in the proposed converter need to sustain a voltage equal to the input voltage $V_{\rm in}$, which is one third of the output voltage.

Fig. 5(a) is used to help determine the voltage rating of the switches. Due to the complimentary operation of the two steps, at any time instance, there will be two switches in the ON state and the other two will be in the OFF state within one stage. For example, Fig. 5(a) shows that in the top stage, S_1 and S_2 are turned ON while S_3 and S_4 are turned OFF. Fig. 5(a) also shows the case that along the dotted path, S_3 and S_9 are in the OFF state and they need to block a voltage difference of 2 $V_{\rm in}$. As a result, each of these two switches needs to sustain a voltage stress of $V_{\rm in}$. Similar analysis can be applied to other switches and the result shows that all eight switches in the top and bottom stages have a voltage stress of $V_{\rm in}$. If the switches with a voltage rating of $V_{\rm in}$ are used in the top and bottom stages, then the switches in the middle stage can theoretically have zero voltage rating since the voltage difference between the middle stage and other stages is only one times $V_{\rm in}$, which can be fully blocked by the switches in the top or bottom stages.

The fact that the switches in the middle stage can have zero voltage stress leads to two other voltage tripler structures with reduced component counts. One has only two switches and no capacitor in the middle stage, as shown in Fig. 5(b). In this structure, the input current interleaving can still be achieved with small degradation compared to the voltage tripler proposed in Fig. 4(a). The output voltage interleaving will not be available since the middle stage output capacitor is not having a 120° shifted with the other two output capacitors.

Another topology is shown in Fig. 5(c). There are no components in the middle stage for this structure, and the voltage source is directly connected to the output capacitor in the

middle stage. Although no interleaving can be achieved, the input current ripple can still be reduced since one third of the energy is directly sent from the source to the load. Compared to the MMCCC [9] circuit, the input current ripple is reduced by 1/3 and the size of the input capacitor can be reduced by more than one half.

IV. Functional Analysis of a Practical Converter With Proposed Structure

The waveforms shown in Fig. 4(c) are obtained under ideal conditions where the duty ratios of the first and second steps have the same value of 0.5. However, because of the structural difference between the first and second step, in order to achieve the 0.5 duty ratio, the required capacitance of the output capacitors needs to be larger than that of the intermediate capacitors, which can increase the total cost of the converter. On the other hand, if output capacitors with the same capacitance as the intermediate capacitors are used, the interleaving function will still be available with only small degradations. In this section, a practical converter with identical capacitance, which is assumed to be C, for all the capacitors, will be analyzed.

A. Soft-Switching Analysis

There are two structural differences between the two charging steps. The first difference is that during the first step, only the intermediate capacitor resonates with the stray inductance of the charging loop. While during the second step, both the intermediate and the output capacitor are in the charging loop. Therefore, the equivalent capacitance of the second step will be a result of two capacitors connected in series, which generates a larger oscillation frequency than the first step. The second difference is that during the second charging step, the intermediate capacitor has to provide both the charging current for the output capacitor and the load current I_D. As a result, if the current needs to be zero before the switches are turned OFF, the angle span of the charging current has to be larger than 180° to offset the extra load current.

Fig. 6 is used to determine the exact duty ratio of the two steps. In this analysis, the stray inductances in the charging loop of the first and second steps are assumed to be the same. In Fig. 6(a), if S_3 and S_4 are turned ON, the following relationship can be established:

$$\begin{cases} V_{C1}(t) - V_{C4}(t) = L\dfrac{di_{S3}(t)}{dt} \\ i_{C4}(t) = -C\dfrac{dV_{C4}(t)}{dt} \\ i_{S3}(t) = C\dfrac{dV_{C1}(t)}{dt} \\ i_{S3}(t) = i_{C4}(t) + I_D. \end{cases} \tag{10}$$

Get the derivative of the first equation in (10)

$$\frac{d(V_{C1}(t) - V_{C4}(t))}{dt} = L\frac{d^2 i_{S3}(t)}{dt^2}. \tag{11}$$

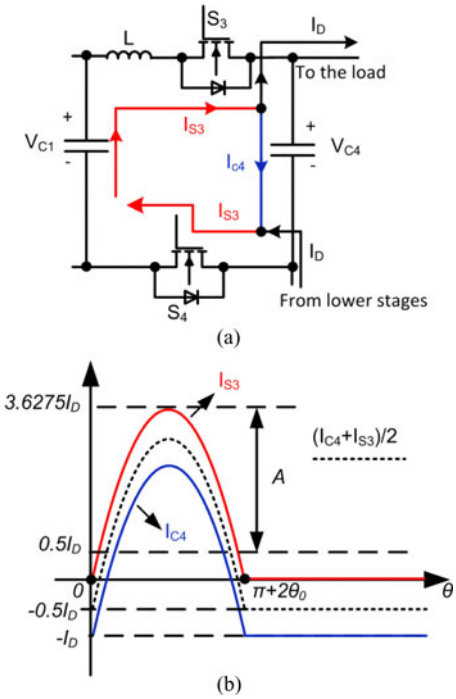

Fig. 6. (a) Current flow in the second step. (b) Current waveforms of S_3 and C_4.

Then, the middle two equations of (10) are substituted into (11), and the following equation is derived:

$$\frac{i_{C4}(t) + i_{S3}(t)}{C} = L\frac{d^2 i_{S3}(t)}{dt^2}. \tag{12}$$

By assuming that the load current changes much slower than the switching frequency, we have

$$\frac{d^2 i_{S3}(t)}{dt} = \frac{d^2 i_{C4}(t)}{dt}. \tag{13}$$

So (12) can be rewritten as

$$i_{S3}(t) + i_{C4}(t) = \frac{1}{2}CL\left(\frac{d^2(i_{S3}(t) + i_{C4}(t))}{dt^2}\right). \tag{14}$$

The pattern of (14) shows that the sum of $i_{S3}(t)$ and $i_{C4}(t)$ is a sinusoidal waveform with an oscillation frequency $\omega_2 = \sqrt{2}/\sqrt{LC}$. If the amplitude is assumed to be $2A$, $i_{S3}(t) + i_{C4}(t)$ can be expressed as

$$i_{S3}(t) + i_{C4}(t) = 2A\sin(\omega_2 t + \varphi). \tag{15}$$

Then, i_{S3} and i_{C4} can be calculated using

$$i_{S3} = A\sin(\omega_2 t + \varphi) + I_D/2 \tag{16}$$

$$i_{C4} = A\sin(\omega_2 t + \varphi) - I_D/2. \tag{17}$$

Given the boundary conditions that the current at the beginning and end of the charging process are both zero

$$\begin{cases} A\sin(\varphi) = \dfrac{-I_D}{2} \\ A\sin(\omega T_2 + \varphi) = \dfrac{-I_D}{2} \end{cases} \tag{18}$$

where $\varphi < 0$ and $\pi/2 < \omega T_2 + \varphi < \pi$, T_2 is the turn ON time of the switches in the second step. Correspondingly, the turn ON time of the switches in the first step should be $T_1 = \pi\sqrt{LC}$.

To fulfill (18), $\omega T_2 + \varphi = \pi - \varphi$, let $\theta_0 = -\varphi$, so

$$T_2 = (\pi + 2\theta_0)\frac{1}{\omega} = (\pi + 2\theta_0)\frac{\sqrt{LC}}{\sqrt{2}}. \tag{19}$$

Then, the duty ratio of the two steps can be calculated as

$$\frac{D_1}{D_2} = \frac{T_1}{T_2} = \frac{\sqrt{2}\pi}{(\pi + 2\theta_0)}. \tag{20}$$

Because the sum of D_1 and D_2 equals 1

$$D_1 = \frac{2\pi}{2\pi + \sqrt{2}(\pi + 2\theta_0)}, \quad D_2 = \frac{\sqrt{2}(\pi + 2\theta_0)}{2\pi + \sqrt{2}(\pi + 2\theta_0)}. \tag{21}$$

To determine the value of θ_0, the conservation of electric charge is used

$$\frac{D_2 \times 2\pi}{\pi + 2\theta_0}\int_{-\theta}^{\pi+\theta}\left(A\sin(\theta - \theta_0) + \frac{I_D}{2}\right)d\theta = 2\pi I_D. \tag{22}$$

By solving this equation, *A* can be expressed as

$$A = \left(\frac{1}{D_2} - \frac{1}{2}\right)\frac{(\pi + 2\theta_0)I_D}{2\cos\theta_0}. \tag{23}$$

Substituting (23) into (18), and noticing that $\theta_0 = -\varphi$

$$((\sqrt{2} + 0.5)\pi + \theta_0) \times \tan\theta_0 = 1. \tag{24}$$

Solving this, $\theta_0 = 9.20^\circ,\ A = 3.1275I_D$. Substituting the result into (16) and (23), the current of S_3 can be written as

$$I_{S3} = 3.1275I_D\sin(\omega t - 9.20^\circ) + I_D/2 \tag{25}$$

$$\frac{D_1}{D_2} = \frac{\sqrt{2}\pi}{(\pi + 2\theta_0)} = 1.283. \tag{26}$$

As a result, the charging duty ratio of the two steps is $D_1 = 0.562,\ D_2 = 0.438$. This will generate a slightly larger conduction power loss compared to the ideal case where both steps have the same duty ratio of 0.5. Using (9), the result shows an increase in the conduction loss of 0.6%, which is negligible. The peak values of the switch currents in the first and second step are $2.795I_D$ and $3.6275I_D$, respectively. Adding a deadtime will not change the ratio between D_1 and D_2 but it will change their absolute values.

To reach the 0.5 duty ratio for both stages, the loop capacitance in the second step C_X needs to be $C_X = (\pi^2/(\pi + 2\theta_0)^2)C \approx 0.8C$. As a result, the output capacitance needs to be $C_{\text{out}} = 4C$, which will significantly increase the cost. For this reason, the output capacitance remains the same as the intermediate capacitors in this analysis.

B. Input Current Interleaving Analysis

Since the duty ratio of the charging current in the first step is 0.562, the interleaving results will be affected. To analyze the interleaving results under this nonoptimum condition, the first-step charging currents of the top stage can be represented by

$$I_1 = \begin{cases} 2.795I_D\sin\left(\dfrac{\theta}{1.124}\right), & 0 < \theta < 1.124\pi \\ 0, & 1.124\pi < \theta < 2\pi. \end{cases} \tag{27}$$

If the converter is running without any interleaving operation and the three stages operate with no phase shift, the input current ripple of the converter is three times the ripples of the top stages. The RMS value of the input current ripple can be calculated using

$$\begin{aligned} &I_{\text{ripple\_rms}} \\ &= \frac{3}{2\pi}\sqrt{\int_0^{1.124\,\pi}\left(2.795I_D\sin\frac{\theta}{1.12} - I_D\right)^2 d\theta + 0.876\pi I_D^2} \\ &= 1.314I_D. \end{aligned} \tag{28}$$

Assuming the ESR of the input capacitor to be R_{C_in}, the power loss on the input capacitor can be calculated using

$$P_{\text{ripple\_rms}} = I_{\text{ripple\_rms}}^2 R_{C\_\text{in}} = 1.727I_D^2 R_{C\_\text{in}}. \tag{29}$$

If the proposed interleaving scheme is adopted, the first-step charging current, in each of the three stages, will still have the same amplitudes and shapes, but with 120° phase shift in between. The resultant input current has a frequency three times the switching frequency. The equations for the first interval $(0 < \theta < 2/3\pi)$ are

$$I_{\text{in\_1}} = \begin{cases} 2.795I_D\sin\left(\dfrac{\theta + 60^\circ}{1.124}\right)\cos\left(\dfrac{60^\circ}{1.124}\right), & 0 < \theta < 0.457\pi \\ 2.795I_D\sin\left(\dfrac{\theta}{1.124}\right), & 0.457\pi < \theta < \dfrac{2}{3}\pi. \end{cases} \tag{30}$$

The RMS value of the input current ripple and corresponding input capacitor power loss can be calculated from (30). The results of the case where the output capacitance equals the intermediate capacitance are shown in the first row of Table I. Here, the RMS values of the input current ripple and the input capacitor power loss are normalized to their value for the same converter without interleaving. It can be seen that the ripple is reduced to less than 1/5 of the original value and the power loss on the input capacitor is reduced to only 3.15% of the original value.

Table I also shows the interleaving results at different output capacitances. The output capacitance is normalized with respect to the capacitance of the intermediate capacitors. It can be seen that by increasing the output capacitance, the duty ratio of the first step can be reduced and the interleaving results can be improved. The loss on the input capacitor will be reduced to less than 1% of the original value if the output capacitance is three or four times the capacitance on the intermediate capacitors. However, the cost will also increase and the benefits of the interleaving are limited.

TABLE I
NORMALIZED INPUT CURRENT RIPPLE AND POWER LOSS AT DIFFERENT OUTPUT CAPACITANCES

Normalized capacitance of output capacitors	Duty ratio of the first step	Relative input current ripple (RMS value)	Relative power loss on the input capacitor
1	0.562	17.75%	3.15%
2	0.524	11.50%	1.32%
3	0.508	9.66%	0.93%
4	0.500	9.59%	0.92%

C. Output Voltage Interleaving Analysis

When the output capacitors are at charging state, the charging current has a sinusoidal shape with an angle span larger than half a cycle and a dc offset is equal to minus half the load current. When they are discharging, their currents are the dc load current. The output capacitor current waveform is shown in the bottom curve of Fig. 6(b). The shape of the capacitor current determines the voltage of each output capacitor. The current on the output capacitor of the top stage can be expressed using

$$I_{C4} = \begin{cases} -I_D, & 0 \le \theta < 2D_1\pi \\ A\sin(B(\theta - 2D_1\pi) - \theta_0)I_D - \dfrac{I_D}{2}, & 2D_1\pi \le \theta < 2\pi. \end{cases} \tag{31}$$

In the case where the capacitance of the output capacitor equals the intermediate one, $A = 3.1275$, $B = (\pi+2\theta_0)/(2\pi D_2) = 1.258$, and $\theta_0 = 9.20^\circ = 0.1606$.

If the initial capacitor voltage at $\theta = 0^\circ$ is assumed to be V_0 and the angular switching frequency is ω, then the capacitor voltage equation can be written as shown (32), at the bottom of this page

To get the maximum and minimum values, the derivative of the capacitor voltage during the second step is calculated

$$\frac{dV_{C4}}{d\theta} = 0 \Rightarrow (A\sin[B(\theta - 2D_1\pi) - \theta_0)] = \frac{I_D}{2}. \tag{33}$$

Solving (33), the two extrema can be derived: $\theta_1 = 2\theta_0/B + 2D_1\pi$ and $\theta_2 = \pi/B + 2D_1\pi$.

The final maximum and minimum points can then be calculated

$$V_{\max} = V_0 - \frac{I_D}{C\omega}\left[2D_1\pi - \frac{2A}{B}\cos\theta_0 + \frac{\pi}{2B}\right] \tag{34}$$

$$V_{\min} = V_0 - \frac{I_D}{C\omega}\left[2D_1\pi + \frac{\theta_0}{B}\right]. \tag{35}$$

Then, the voltage ripple of one output capacitor can be calculated

$$\Delta V_C = V_{\max} - V_{\min} = \frac{I_D}{C\omega}\left[\frac{2A\cos\theta_0 - \pi/2 + \theta_0}{B}\right] = \frac{I_D}{C\omega} \times 3.787. \tag{36}$$

The total output voltage is the sum of the three-stage voltages. The resultant voltage will have a frequency three times that of the switching frequency. So it can be represented using the three-stage voltage at $0 < \theta < 120^\circ$. The voltage can be expressed as shown (37), at the bottom of this page.

The two extremal points of the output voltage can, thus, be calculated as $\theta_1 = (2D_1 + 2/3 - 2)\pi$, $\theta_2 = (2D_1 + 4/3 - 2)\pi$. Then, the voltage ripple of the total output voltage is

$$\Delta V_{C\text{out}} = V_{\max} - V_{\min} = \frac{I_D}{C\omega} \times 0.425. \tag{38}$$

From (36) and (38), it can be seen that the interleaving operation can reduce the total output voltage ripple to around one ninth of the original value. This will effectively reduce the requirement of the output capacitance.

Fig. 7 shows the simulation results for a 55-kW switched-capacitor voltage tripler with the proposed topology. In this simulation, the input voltage and the load current are 200 V and

$$V_{C4} = \begin{cases} V_0 - \dfrac{I_D}{C\omega}\theta, & 0 \le \theta < 2D_1\pi \\ V_0 - \dfrac{I_D}{C\omega}\left\{2D_1\pi + \dfrac{A}{B}\left[\cos(B(\theta - 2D_1\pi) - \theta_0) - \cos\theta_0\right] - \dfrac{1}{2}(\theta - 2D_1\pi)\right\}, & 2D_1\pi \le \theta < 2\pi. \end{cases} \tag{32}$$

$$V_{\text{out}} = \begin{cases} 3V_0 - \dfrac{I_D}{C\omega}\left\{2.5\theta + \left(2D_1 + \dfrac{2}{3}\right)\pi - \dfrac{\theta_1}{2} + \dfrac{A}{B}\left[\cos(B(\theta - \theta_1) - 0.1606) - \cos(\theta_0)\right]\right\}, & 0 < \theta < 2D_1\pi/3 \\ 3V_0 - \dfrac{I_D}{C\omega}\left\{2\theta + 4D_1\pi - \dfrac{(\theta_1 + \theta_2)}{2} + \dfrac{A}{B}\left[\begin{matrix}\cos(B(\theta - \theta_1) - 0.1606) \\ +\cos(B(\theta - \theta_2) - 0.1606) - 2\cos(\theta_0)\end{matrix}\right]\right\}, & 2D_1\pi/3 < \theta < 2\pi/3. \end{cases} \tag{37}$$

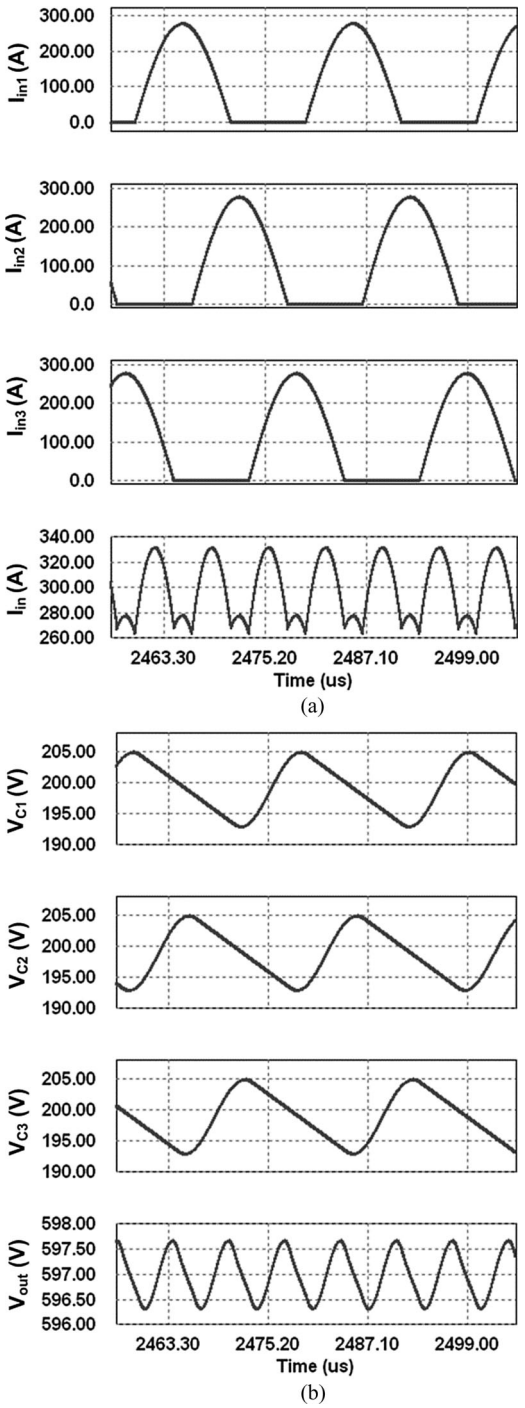

Fig. 7. Simulation results of a 55-kW switched-capacitor voltage tripler. (a) Input current $I_{\rm in}$ and the charging current of three stages $I_{\rm in1}$, $I_{\rm in2}$, and $I_{\rm in3}$. (b) Total output voltage $V_{\rm out}$ and the voltages on the three output capacitors.

100 A, respectively. The capacitance of each capacitor is assumed to be 100 μF and the switching frequency is set to 50 kHz. Under this switching frequency, the loop stray inductance needs to be at least 100 nH to achieve the adopted soft-switching scheme. With the development of SiC and GaN technologies, devices with higher switching speed and greater voltage blocking capability should become affordable in the near future. The increase of switching frequency will largely reduce the requirement on the stray inductance of the charging loops.

TABLE II
COMPARISON BETWEEN THE INTERLEAVING MMCCC CIRCUIT AND PROPOSED TOPOLOGY

Topology	Interleaving ZCS-MMCCC	Proposed converters
No. of capacitors	9	6
Voltage rating of capacitors	V_{in},$2V_{in}$ and $3V_{in}$	V_{in}
No. of switches	21	12
Voltage rating of switches	V_{in} or $2V_{in}$	V_{in}
Current rating of each capacitors and switches	$I_D/3$	I_D
Total No. of base capacitors	14	6
Total No. of base switches	8	12

Using (36), each individual capacitor has a peak-to-peak voltage ripple of 12.06 V. However, the total output voltage ripple is fairly small, which is around 1.35-V peak to peak. Fig. 7(a) shows the current interleaving results and Fig. 7(b) shows the voltage interleaving results. The simulation results in Fig. 7 verify the aforementioned calculations.

D. Comparison Between the Proposed Circuit and the Interleaving ZCS-MMCCC Circuit

Table II shows the comparison between the interleaving ZCS-MMCCC [11] and the proposed circuit. Note that in [11], the term "ZCS multilevel modular switched-capacitor dc-dc converter (ZCS-MMSCC)" is used instead of ZCS-MMCCC. However, the term "ZCS-MMCCC" is used here to maintain the consistency with the previous content in this paper.

In this comparison, soft switching and interleaving are assumed to be realized in both topologies. The first and third rows of Table II show the number of capacitors and switches required for each topology. It can be seen that the numbers of both capacitors and switches are smaller in the proposed topology compared to the interleaving ZCS-MMCCC topology.

The last two rows of Table II take both the component count and the component stress into consideration. Here, the "base capacitor" and "base switch" concepts are used to make comparisons. One base capacitor is defined to have a voltage rating of $V_{\rm in}$ and a capacitance that satisfies the voltage drop requirements in one switching cycle. One base switch is defined to have a voltage rating of $V_{\rm in}$ and current rating of I_D. It can be seen that the proposed circuit employs far fewer capacitors than the interleaving ZCS-MMCCC circuit. This is because the sizing of capacitors has a square relationship versus their voltage stress. For example, to realize a capacitor with 3-$V_{\rm in}$ rating while keeping the capacitance the same, a total of nine capacitors with a rating of $V_{\rm in}$ are needed. Since the capacitors in the proposed topology are all rated at $V_{\rm in}$, while the ZCS-MMCCC topology employs capacitors with higher capacitor ratings, a smaller number of capacitors are expected for the proposed topology.

On the other hand, the total number of switches for the proposed converter is larger than that of the interleaving ZVS-MMCCC circuit. This is due to the fact that the current in the interleaving ZCS-MMCCC is separated into three identical

TABLE III
DUTY RATIO AT DIFFERENT STRAY INDUCTANCE RATIOS

L_1/L_2	D_1	D_2
1.1	0.578	0.422
0.9	0.547	0.452
0.8	0.531	0.469
0.7	0.513	0.486
0.6	0.499	0.501

voltage triplers, so the current stress of each switch is 1/3 of its original value. However, due to the large number of switches required by the interleaving ZCS-MMCCC circuit, the cost of the switches may not be lower than the proposed circuit and the chance of switch failure is much higher.

E. Influence of Unequal Stray Inductances of the Two Steps

The aforementioned analysis assumed that the stray inductances of the two steps are the same. However, this may not always be the case in the practical design. The difference of stray inductances affects the duty ratios of the two steps to achieve soft switching. If the stray inductances of the first step and second step are assumed to be L_1 and L_2, respectively, then the values of D_1 and D_2 are determined by the ratio of L_1 to L_2.

Table III shows the duty ratio of the two steps at different values of L_1/L_2, which is calculated under the assumption that the capacitance of the output capacitor equals the intermediate capacitor. It can be seen that if L_1/L_2 equals 0.6, the duty ratio of both steps is close to 0.5 and the converter can have best interleaving results. This feature can be used in practical converter design.

V. EXPERIMENTAL RESULTS

A 2-kW switched-capacitor voltage tripler prototype using a group of multipurpose switched-capacitor testing boards has been built to verify the ideas presented in this paper. Each test board contains four switches and two capacitors, but only two switches and one capacitor are used in this experiment. Therefore, a total of six boards are employed to build the voltage tripler.

Ten C5750×7R2A475 K ceramic capacitors with a voltage rating of 100 V and a capacitance of 4.7 μF are put in parallel to form one main capacitor. At a switching frequency of 80 kHz and a load current of 25 A, the voltage ripple on the capacitors is around 5 V. Note that, for ceramic capacitors, the capacitance variation with their operation voltage can be as high as 40%. Therefore, film capacitors should be used in a better design to achieve a stable oscillation frequency.

Different test boards are connected through external cables. The cable lengths are made the same, so the stray inductances of different charging loops are similar. To calculate the stray inductance of each charging loop, the oscillation frequencies are measured at a capacitor voltage of 5 V. The measured oscillation

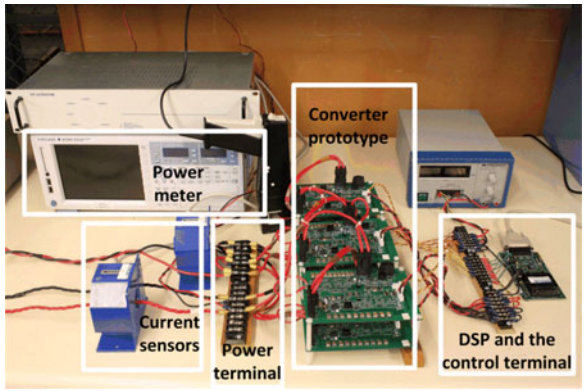

Fig. 8. Test setup of the experiment.

frequencies of the three first-step charging currents (from the top stage to the bottom stage) are 63.4, 65.7, and 65.1 kHz, respectively. The corresponding loop inductances are calculated to be 134, 125, and 127 nH, respectively.

Three IRFI4410ZPbF MOSFETs are connected in parallel to form a single switching device. The on-resistance of each MOSFET is 10 mΩ. The printed circuit board traces in the charging loop add another 7–8 mΩ resistance, so the total loop resistance is around 15 mΩ and the damping factor is around 0.15.

To control the proposed voltage tripler, three complementary signals with 120° phase shift in between are needed. A 200-nS deadband is added between two complimentary signals to avoid the shoot-through. A TI TMS320F2812 DSP is used as the main controller.

Fig. 8 shows the test setup of the experiment. The duty ratios of the first and second steps are 0.466 and 0.520, respectively. At a 50-V input voltage, soft switching is achieved for both steps at a switching frequency of 72.0 kHz. Since the surface area of this prototype is large, the heatsink is not needed during the test.

Fig. 9 shows the input current interleaving effect at a load current of 10 A. The lower three waveforms are the charging current I_{S1}, I_{S5}, and I_{S9} of the three stages in the first step. The peak values of the I_{S1}, I_{S5}, and I_{S9} are 31.6, 30.8, and 31.0 A, respectively. Both I_{S5} and I_{S9} drop to 0.2 A when their corresponding switches are turned OFF, demonstrating that ZCS is well achieved. However, when S_1 is turned OFF, the value of I_{S1} is -1.6 A. The reason is that the charging loop of I_{S1} has a larger stray inductance than the other two charging loops.

The top two waveforms in Fig. 9 are the sum of the three charging currents ($I_{S1} + I_{S5} + I_{S9}$) and the input current $I_{\rm in}$, respectively. The sum of the three charging currents has a peak-to-peak ripple 14.6 A and an RMS ripple of 2.95 A. This RMS ripple value corresponds to 22.4% of the ripple if no interleaving method is used in this topology. Based on Table II, if the stray inductances of the three stages are the same, the RMS value of the current ripple should be 17.75% of the case when no interleaving method is used. This shows that the variation of parameters can affect the interleaving results. A 47-μF input capacitor is used to filter out the input current ripple. It can be

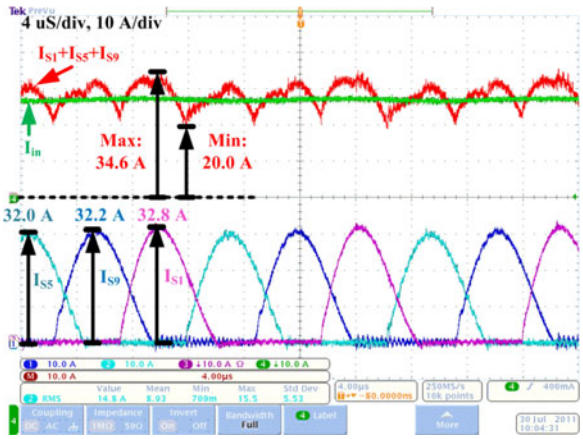

Fig. 9. Input current interleaving results.

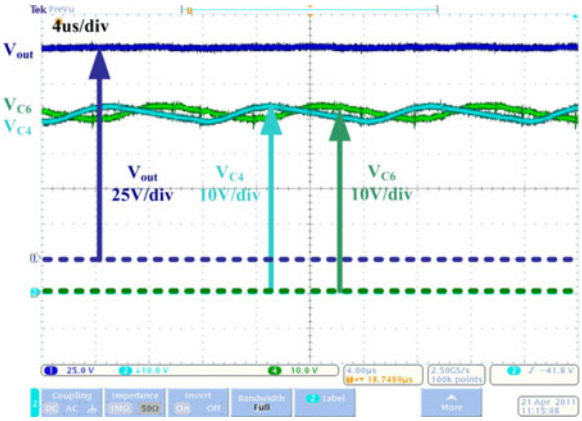

Fig. 10. Output voltage interleaving results.

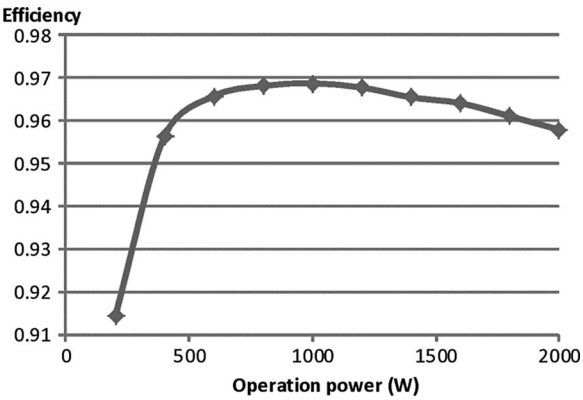

Fig. 11. Efficiency curve of the proposed converter.

seen that the input current has very small ripple on it, with an RMS value of 0.456 A.

Fig. 10 shows interleaving results of the output voltage. The lower two waveforms are the output capacitor voltage of the top (V_{C4}) and bottom (V_{C6}) stage, respectively. They have a peak-to-peak voltage ripple of 6 V. The top waveform is the total output voltage, which has a voltage ripple less than 1 V.

Fig. 11 shows the efficiency of the prototype over the operation range from 200 to 2000 W with 50-V input voltage. It is measured using a Yokogawa WT3000 power meter. Two LEM Danfysik IT-700s high-performance closed-loop current transducers are utilized to ensure measurement accuracy. The control power loss is separately measured from the control power supply and added to the total loss.

The efficiency is higher than 96% for most of the test range. It should be noted that since different testing boards are connected through external cables, the stray inductance is not optimized, which adds to the inaccuracy of soft switching and interleaving and, thus, reduces the efficiency in this test. A dedicated and integrated design can increase the total efficiency of the converter.

VI. Conclusion

A switched-capacitor voltage tripler with interleaving capability is presented in this paper. This converter possesses the advantage of minimized intermediate capacitor stages, 50% duty ratio for the charging current, soft switching, and interleaving capability without additional components. Detailed structural and functional analyses are performed. The experimental results on a 2-kW prototype verified the proposed topology. This circuit can be utilized in applications ranging from subkilowatt to many hundreds of kilowatts with the advantage of low input current and output voltage ripple, low volume, and high efficiency.

References

[1] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits Syst. Mag.*, vol. 1, no. 3, pp. 37–42, Third Quarter 2001.

[2] H. Chung, "Design and analysis of a switched-capacitor-based step-up dc–dc converter with continuous input current," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 46, no. 6, pp. 722–730, Jun. 1999.

[3] H. S. Chung, A. Ioinovici, and W. Cheung, "Generalized structure of bi-directional switched-capacitor dc–dc converters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 6, pp. 743–753, Jun. 2003.

[4] F. L. Luo and H. Ye, "Positive output multiple-lift push–pull switched-capacitor Luo-converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 594–602, Jun. 2004.

[5] B. Arntzen and D. Maksimovic, "Switched-capacitor DC–DC converters with resonant gate drive," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 892–902, Sep. 1998.

[6] J. M. Henry and J. W. Kimball, "Practical performance analysis of complex switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 127–136, Jan. 2011.

[7] F. Z. Peng, F. Zhang, and Z. Qian, "A magnetic-less DC–DC converter for dual-voltage automotive systems," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 511–518, Mar. 2003.

[8] W. Qian, F. Z. Peng, and L. M. Tolbert, "Development of a 55 kW 3X DC–DC Converter for HEV systems," in *Proc. Veh. Power Propulsion Conf.*, 2009, pp. 433–439.

[9] F. H. Khan and L. M. Tolbert, "A multilevel modular capacitor-clamped DC–DC converter," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1628–1638, Nov. 2007.

[10] F. H. Khan, L. M. Tolbert, and W. E. Webb, "Start-up and dynamic modeling of the multilevel modular capacitor-clamped converter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 519–531, Feb. 2010.

[11] D. Cao and F. Z. Peng, "Multiphase multilevel modular DC–DC converter for high-current high-gain TEG application," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1400–1408, May/Jun. 2011.

[12] S. Tan, S. Kiratipongvoot, S. Bronstein, A. Ioinovici, Y. M. Lai, and C. K. Tse, "Adaptive mixed on-time and switching frequency control of a system of interleaved switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 364–380, Feb. 2011.

[13] K. Zou, M. J. Scott, and J. Wang, "Switched-capacitor cell based DC–DC and DC–AC converters," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2011, pp. 224–230.

[14] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.
[15] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, "A new design method for high-power high efficiency switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 832–840, Mar. 2008.
[16] K. K. Law, K. W. E. Cheng, and Y. P. B. Yeung, "Design and analysis of switched-capacitor-based step-up resonant converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 5, pp. 943–948, May 2005.
[17] M. Shoyama, F. Deriha, and T. Ninomiya, "Operation analysis and control of resonant boost switched-capacitor converter with high efficiency," in *Proc. Power Electron. Spec. Conf.*, 2005, pp. 1966–1971.
[18] J. Kimball, P. Krein, and K. Cahill, "Modeling of capacitor impedance in switching converters," *IEEE Power Electron. Lett.*, vol. 3, no. 4, pp. 136–140, Dec. 2005.
[19] K. Sano and H. Fujita, "Performance of a high-efficiency switched-capacitor-based resonant converter with phase-shift control," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 344–354, Feb. 2011.
[20] D. Cao and F. Z. Peng, "A family of zero current switching switched-capacitor dc–dc converters," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2010, pp. 1365–1372.
[21] Z. Pan, F. Zhang, and F. Z. Peng, "Power loss and efficiency analysis of multilevel DC–DC converters," in *Proc. 20th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2005, pp. 1393–1398.
[22] P. K. Peter and V. Agarwal, "Analysis and design of a ground isolated switched-capacitor DC–DC converter," in *Proc. IEEE Int. Symp. Ind. Electron.*, Bari, Italy, Jul. 2010, pp. 632–637.

Ke Zou (S'09) received the B.S. and M.S. degrees from Xi'an Jiaotong University, China, in 2005 and 2008, respectively. He is currently working toward the Ph.D. degree at the Ohio State University.

His current research projects and topics include switched capacitor dc/dc converter and dc/ac multilevel inverter, battery model in high frequency application and hardware in the loop (HIL) systems for power electronics and power systems.

Mark J. Scott (S'09) received the B.S. degree in electrical and computer engineering in 2005 from Ohio State University, Columbus, where he is currently working toward the Ph.D. degree in electrical and computer engineering since 2009.

He has worked as a Field Engineer installing large industrial automated systems and as a Test Engineer validating power electronics for automotive applications. His research is focused on utilizing wide bandgap devices in new and existing power electronic topologies for renewable energy applications.

Mr. Scott is a founding member of the IEEE Graduate Student Body at the Ohio State University and a member of Tau Beta Pi.

Jin Wang (S'02–M'05) received the B.S. degree from Xi'an Jiaotong University, China, in 1998, the M.S. degree from Wuhan University, China, in 2001, and the Ph.D. degree from Michigan State University, East Lansing, in 2005, all in electrical engineering.

From September, 2005 to August 2007, he worked at the Ford Motor Company as a Core Power Electronics Engineer and contributed to the traction drive design of the Ford Fusion Hybrid. Since September 2007, he has been an Assistant Professor in the Department of Electrical and Computer Engineering at Ohio State University, Columbus. His teaching position is co-sponsored by American Electric Power, Duke/Synergy, and FirstEnergy. He has over 40 peer-reviewed journal and conference publications. His research interests include high-voltage and high-power converter/inverters, integration of renewable energy sources, and electrification of transportation.

Dr. Wang received the IEEE Power Electronics Society Richard M. Bass Young Engineer Award and the National Science Foundation's CAREER Award, both in 2011. He has been an Associate Editor for IEEE TRANSACTIONS ON INDUSTRY APPLICATION since March 2008.