A High Boost Ratio Bidirectional Isolated dc-dc Converter for Wide Range Low Voltage High Current Applications

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***Abstract* — This paper introduces a high boost ratio, bidirectional, isolated, dc/dc converter designed as an interface between low voltage, high current dc sources and 24 V dc systems. This converter realizes bidirectional power flow with two main switches and operates under a wide input voltage range, from 1.5 V to 12 V, with an input current as high as 300 A. An active snubber circuit is utilized to recycle the energy stored in the leakage inductor of transformer and realize zero voltage switching (ZVS) off for one main switch. The zero current switching (ZCS) on of this switch is achieved by using transformer leakage inductor, thus no additional components are needed. Furthermore, the power loss of another main switch is minimized by operating it in the Synchronous Rectification mode. Complete circuit description and operation principles are provided in this paper. A 1.2 kW lab prototype has been built and tested with full power rating. Both simulation results and experimental results are presented to verify proposed functions.**

I. INTRODUCTION

Many low voltage high current dc sources, like ultra capacitor banks, Li - Ion batteries and NiMH batteries require high boost ratio dc/dc converters to transfer their energy into higher dc systems. However, it is challenging to design a universal interface between these types of dc sources and higher voltage systems because of the large variation of input voltage and the high current requirement. Based on the survey of existing products of ultra capacitors, Li - Ion and NiMH batteries, the designed targets of the converter include:

- input voltage range: 1.5 V to 12 V;
- maximum current: 300 A (from 2 V to 4 V);
- minimum output voltage at 24 V, which is a common voltage rating in electric power steering systems.
- bidirectional power flow capability.

There are a lot of applications in low voltage high current dc/dc energy conversion area, but most of them are designed for fuel cell and automotive electrical systems, which have different operation conditions. For fuel cell applications, many papers are focused on the Solid Oxide Fuel Cell which can operate from 22 V to 41 V, with 5 kW continuous power [1-2]. In automotive area, due to the increasing demand for electrical power, 42 V electrical distribution systems have been seen in hybrid electric vehicles together with the traditional 14 V system. Thus, a 42 V /14 V, 2 kW – 5 kW dc/dc converter is needed and a lot of researches have been carried out on this topic [3-5].

However, for the lower voltage range addressed in this paper, only limited publications have been presented [6-8]. One of the major challenges in this topic is the difficulty to realize high efficiency under such a low voltage and high current rating. Taking the example of Energy Star Program's 80 PLUS standard, till now many manufacturers still do not have products that could be certified for 80 PLUS Silver level, which requires efficiency higher than 85% [9-11]. Compared with server power supplies, the proposed converter design is facing tougher challenges: 1) extremely low operation voltage, down to 1.5 V; 2) large current capability, up to 300 A; 3) high boost ratio as high as 16; and 4) wide input voltage range; from 1.5 V to 12 V, an eight fold of change.

In practical designs, it is often difficult to use transformerless converters to realize high boost ratio without adding component counts [12]. Furthermore, the large current rating excludes traditional isolated circuit topologies, such as the flyback and forward converters. For commonly used full bridge based converters, each switch is required to handle the full load current. To deliver 300 A, the high switch count and the number of devices in parallel for each switch, will make the circuit economically not feasible. As shown in [13-15], coupled inductor based converters can meet part of the requirements, but at the price of either high circuit complexity or limited current rating.

This paper proposes a cost effective circuit based on isolated Cuk converter [16]. The proposed converter has

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following main features: 1) a wide input voltage range with high current; 2) a high boost ratio; 3) bidirectional power flow capability achieved with only two main switches; 4) an active snubber circuit that improves the efficiency of the circuit for a wide operation range. The active snubber circuit absorbs the energy stored in the transformer leakage inductance and returns it to the source, thus clamping the overshoot voltage during switching transients. 5) soft switching, which is realized by using the active snubber circuit, the stray inductance of transformer and synchronous rectification (SR) operation [17], thereby the overall converter efficiency is improved. Because of the large current rating, MOSFETs are paralleled in this circuit. Thus, a large gate charge is expected. To further improve the efficiency of the circuit, a gate drive circuit with energy recovery function has also been adopted in the circuit design [18].

To ensure better efficiency, a 1.2 kW prototype is built. Both simulation and experimental results are presented at the end of the paper.

II. CIRCUIT DESCRIPTION AND OPERATION PRINCIPLES

A. Circuit Description

Fig. 1 shows the proposed converter. The input side (V_{Low}) is connected to a low voltage, high current bidirectional dc source, the output side (V_H') is connected to a 24 V dc system. The main circuit is an isolated Cuk converter [16], and the two main switches S_1 and S_2' work in a complementary mode. When the power flow is from V_{Low} to V_H', S_2' is operated in the SR mode. When the power flows in another direction, S_1 works in SR mode. With the synchronous rectification, the switches' conduction and switching loss can be decreased. In the circuit diagram, D_1 and D_2' are the body diodes of S_1 and S_2', respectively. For each switch, ten MOSFETs are used in parallel. Due to the complexity of the layout, no external Schottky diodes are used. An active snubber circuit is added to recover the energy stored in the leakage inductance. D_{S1}, D_{S2}, C_{sb1}, L_{sb1} and S_{S1} form the low voltage side active snubber circuit; and D_{S3}', D_{S4}', C_{sb2}', L_{sb2}', S_{s2}' form the high voltage side active snubber circuit.

B. Operation Principles

If the power flow is from V_{Low} to V_H', the high voltage side snubber circuit will not influence the circuit operation, and S_{S2}' can be disabled. Then the low voltage side referred equivalent circuit is shown in Fig. 2, in which L_S is the leakage inductance of transformer, S_{S1} and S_1 have the same gate signal. Vice verse, when the power changes direction, S_{S1} is disabled and S_{S2}' is controlled in synchronization with S_2'.

The circuit analysis is based on following assumptions: 1) C_1 and C_2 are large enough to keep almost constant v_{C1} and v_{C2}; 2) L_1 and L_2 are large enough to result in negligible ripple currents on L_1 and L_2. For the circuit shown in Fig. 2, at steady state [16]:

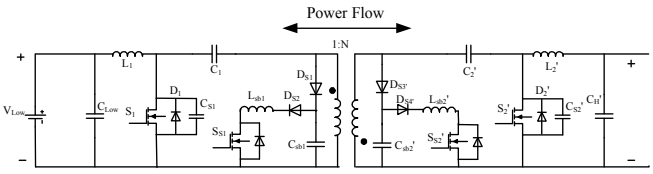


Figure 1. Bidirectional isolated dc/dc converter

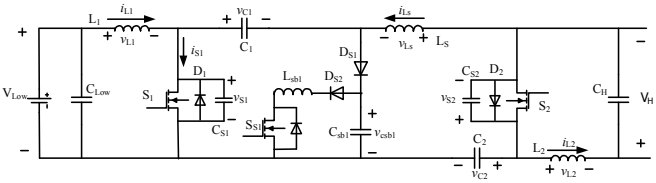


Figure 2. Low voltage side referred equivalent circuit

$$\frac{V_H}{V_{Low}} = \frac{I_{Low}}{I_H} = \frac{D}{1-D}, \quad (1)$$

$$v_{C1} = V_{Low}, \text{ and} \quad (2)$$

$$v_{C2} = V_H. \quad (3)$$

where D is the duty ratio of S1.

The main idea behind the snubber circuit is that the energy stored in the leakage inductance will be dumped into the C_{sb1}, during the transient that the switch S_1 and S_{s1} are turned off. The energy recovery of this active snubber circuit is divided into two parts. One part of the energy is recovered through L_{sb1} and another part of energy is returned by C_{sb1}. First, when S_1 and S_{s1} are turned on, there will be resonance between C_{sb1} and L_{sb1}. The voltage on C_{sb1} will change polarity and reach its negative rail $-V_{Low}$. Because the positive rail and negative rail of v_{Csb1} are different, part of the energy stored in C_{sb1} may become residue current of L_{sb1} in the end of the resonance, depends on the the positive and negative rail values of v_{Csb1}. This residue current, if any, will then be absorbed by C_1. Another energy recovery is happened in the next switching cycle. When S_1 and S_{s1} are turned off again, since v_{Csb1} is negative, C_{sb1} will release the energy stored in it to C_1. When v_{Csb1} reaches zero, this energy recovery ends and C_{sb1} begins to absorb energy from the main circuit. If designed and operated correctly, the v_{Csb1} is positive when the switch S_1 and S_{s1} are off; vice versa, v_{Csb1} is negative when S_1 and S_{s1} are on.

The voltage and current waveforms of the main circuit and the snubber circuit are shown in Fig. 3, in which $v_{gs,\,SX}$ represents the gate drive signal for the switch. One complete switching period can be divided into following 9 steps：

Step 1 (0 to t_1): both S_1 and S_{S1} are on, main circuit currents i_{L1} and i_{L2} are flowing through S_1. The input voltage source V_{Low} is charging L_1, main circuit capacitors C_1 and C_2 are charging L_2 and provide power for the load. For active snubber circuit, the residue current on L_{sb1} has reached zero and the energy feedback procedure has finished. Due to the resonance between C_{sb1} and L_{sb1} in earlier step, the voltage on C_{sb1} has already reached its negative rail and been clamped by v_{C1}. In this step, v_{Csb1}= $-v_{C1} = -V_{Low}$, $v_{S2}= v_{L2}+ V_H = V_{Low} + V_H$.

Step 2 ($t_1 - t_2$): at t_1, S_1 is turned off. Since the voltage across S_1 is clamped by C_1 and C_{sb1}, and $v_{Csb1}(t_1) = -v_{C1}$, S_1 is ZVS off. The main circuit currents i_{L1} and i_{L2} begin to flow through C_{sb1}, C_{sb1} will first release the stored energy to C_1 until v_{Csb1} reaches zero. After that this energy feedback stops and C_{sb1} begins to absorb energy from L_1 and L_2. v_{Csb1} keep increasing and reaches V_H at t_2. Since $L_S << L_2$, the voltage on L_S is negligible. Then D_2 is forward biased and starts to conduct current.

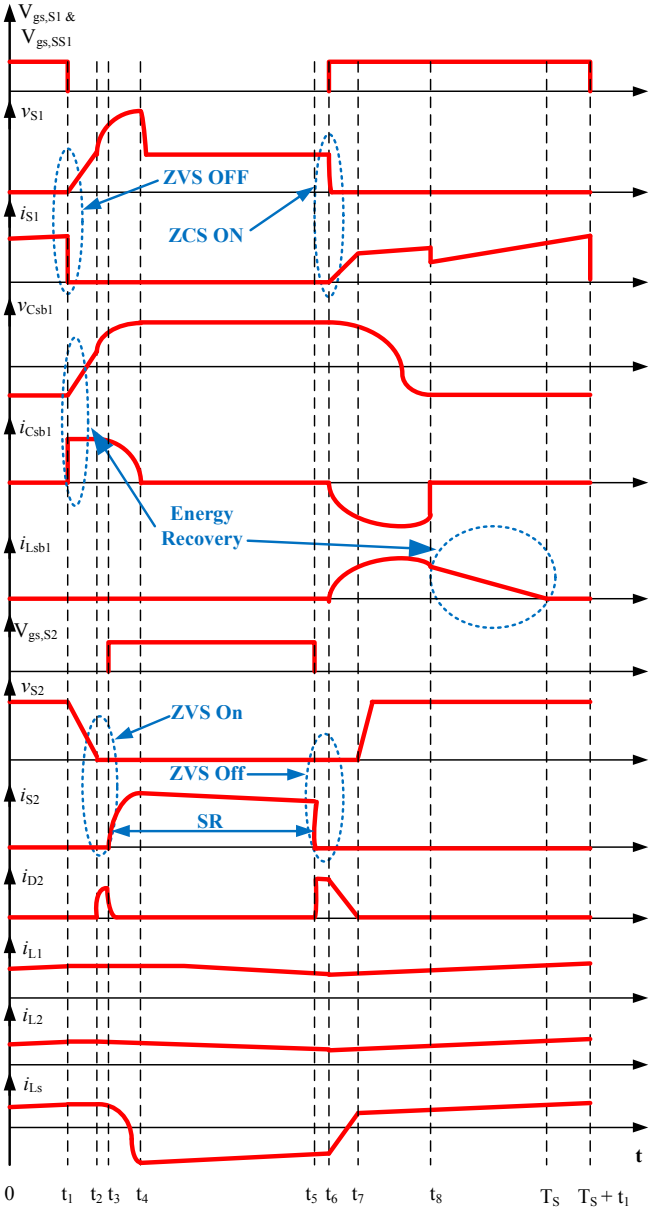


Figure 3. Waveforms of proposed converter

Step 3 ($t_2 - t_3$): at t_2, i_{L2} begins to go through D_2, v_{S2}=0.

Step 4 ($t_3 - t_4$): at t_3, the deadtime is over and S_2 is ZVS on. Since S_2 has lower resistance than D_2, S_2 will take over the current and work in the SR mode. In this time interval, both i_{L1} and i_{Ls} will keeping charging C_{sb1}. i_{Ls} is decreasing and finally changes polarity. At t_4, i_{Ls} has the same amplitude and direction with i_{L1}, v_{Csb1} reaches its positive rail $v_{Csb1\_initial}$, and $v_{S1}(t_4) = v_{C1}(t_4) + v_{Csb1}(t_4) = V_{Low} + v_{Csb1\_initial}$.

Step 5 ($t_4 - t_5$): both i_{L1} and i_{L2} are flowing through S_2. The current on D_{S1} has reached zero and D_{S1} is reversed biased. The voltage on S_1 is clamped by C_1, L_S and C_2. Because $L_S << L_1$, $v_{Ls} \approx 0$, then $v_{S1} \approx v_{C1} + v_{C2} = V_{Low} + V_H$.

Step 6 ($t_5 - t_6$): at t_5, S_2 is ZVS off, and both i_{L1} and i_{L2} will go through D_2.

Step 7 ($t_6 - t_7$): at t_6, the deadtime is over and S_1 and S_{S1} are turned on. Since $v_{Ls} = v_{C1} + v_{C2} = V_{Low} + V_H$, i_{Ls} will increase from $-i_{L1}$, and S_1 is ZCS on because $i_{S1} = i_{L1} + i_{Ls}$. In the active snubber circuit, resonant inductor L_{sb1} will clamp the change current through S_{S1}, so S_{S1} is also ZCS on. Then, C_{sb1} begins to resonate with L_{sb1}, and v_{Csb1} is decreasing.

Step 8 ($t_7 - t_8$): at t_7, both i_{L1} and i_{L2} are flowing through S_1, there is no current flowing through D_2. The voltage on D_2 is clamped by C_1, L_S and C_2. Since $i_{Ls} = i_{L2}$, and i_{L2} has negligible ripple, $v_{Ls} \approx 0$, then $v_{D2} = v_{C1} + v_{C2} = V_{Low} + V_H$, D_2 is reverse biased. In the active snubber circuit, v_{Csb1} keep decreasing. At t_8, v_{Csb1} reaches $-v_{C1}$ and is clamped to be $-v_{C1}$ by D_1 and D_{S1}.

Step 9 ($t_8 - T_S$): at t_8, since v_{Csb1} is clamped to be $-v_{C1}$, the residue current on L_{sb1}, if any, will flow through D_1, C_1, D_{S1}, D_{S2} and start to charge C_1. This energy feedback will introduce a drop of i_{S1}. At T_S, the current on L_{sb1} reaches zero, the energy recovery procedure ends, circuit will repeat step 1.

Based on above analysis, the two step energy recovery function of the active snubber circuit can be summarized as following: Before S_{S1} is turned off, v_{Csb1} has already been clamped to be $-V_{Low}$. Then S_1 and S_{S1} are both turned off, i_{L1} and i_{L2} will go through C_{sb1}, C_{sb1} will release energy to C_1 until v_{Csb1} reaches zero. After that, v_{Csb1} will keep increasing and finally reaches its positive rail $v_{Csb1\_initial}$. When S_{S1} is turned on again, C_{sb1} will resonate with L_{sb1}, the voltage on C_{sb1} is decreasing and finally reaches its negative rail, which is $-V_{Low}$. Depends on the amplitudes of V_{Low} and $v_{Csb1\_initial}$, part of the energy stored in C_{sb1} may become residue current of L_{sb1} and then be absorbed by C_1.

The designed circuit also has intrinsic soft switching functionality. For example, the ZVS off and ZCS on of S_1 are achieved by utilizing C_{sb1} and L_s; the ZVS off and on of S_2 are realized by the SR operation. Therefore, the overall efficiency is improved.

The low voltage side and high voltage side have symmetric circuit structures, thereby when the power flows in the other direction, the circuit operates in a similar way.

III. DESIGN GUIDELINE

The system requirements are shown in Table 1.

Table 1. THE SYSTEM REQUIREMENTS

V_{Low}	1.5 V to 12 V
I_{Low}	100 A when V_{Low} = 1.5 V 300 A when 2 V ≤ V_{Low} ≤ 4 V (1200/V_{Low}) A when 4 V ≤ V_{Low} ≤ 12 V
V_H	24 V
P_{max}	1.2 kW

A. *Lossless Gate Drive Circuit Design*

For regular gate drive circuit which charge and discharge the MOSFET input capacitor through gate resistors, the power loss in the gate drive circuit will increase with high switching frequency and gate capacitance, sometimes the power loss will be unacceptable due to high components cost and big size. For example, in the prototype, to decrease the conduction loss, 10 IPB019N08N3 MOSFETs are placed in parallel to form S_1. According to the datasheet, for each MOSFET the gate to source capacitance is 14.1 nF. When S_1 is switched at 100 kHz, and V_{gs} is 15 V, the power consumption on the gate resistor would be $P = 10 \times C_{gs} \times V_{gs}^2 \times f = 3.17$ W. Considering the power consumption of other components in the gate drive circuit, the isolated dc/dc power supply in this gate drive circuit needs to supply at least 4 W, which requires components with high cost and large footprint. Therefore, a gate drive circuit with energy feedback capability, shown in Fig. 4 is adopted [18]. In this circuit, the leakage inductance of transformer instead of gate resistor is utilized to limit the gate current. During the turning on and off transients, the current flowing through primary side winding will be recovered back to the power supply through the secondary winding. By selecting a transformer with small leakage inductance, the high switching speed can be easily realized. With this gate drive circuit, a regular 2 W isolated dc/dc power supply chip is more than enough for the whole gate drive circuit.

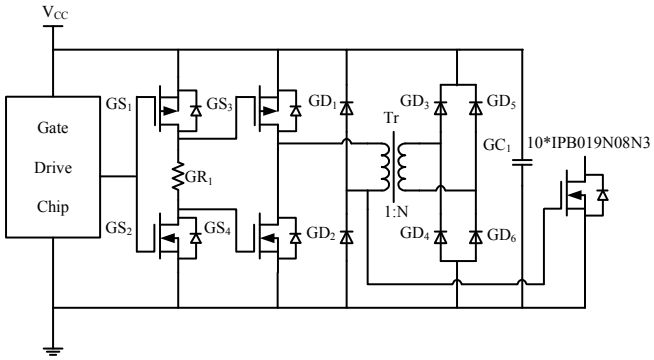


Figure 4. Lossless gate drive circuit

B. *Power Loss Analysis*

For the circuit shown in Fig. 2, the switching loss of S_1 and S_2 can be neglected due to their soft-switching operation.

The conduction loss of the circuit can be classified into three groups: the conduction loss on the switches, on the capacitors and on the magnetic components (inductors and transformers). The current profiles of major components are shown in Fig. 5, and the corresponding equivalent circuits are described in Fig. 6. To simplify the analysis, the currents on L_1 and L_2 are assumed to be constant, and the impact of the energy feedback on S_1 is ignored. Also, based on earlier circuit analysis in step 6, D_2 will take over the current when S_2 is turned off. And the deadtime is very short, the deadtime between the off state of S_2 and the on state of S_1 (from $\delta_6 T_S$ to T_S)will not affect the circuit operation.

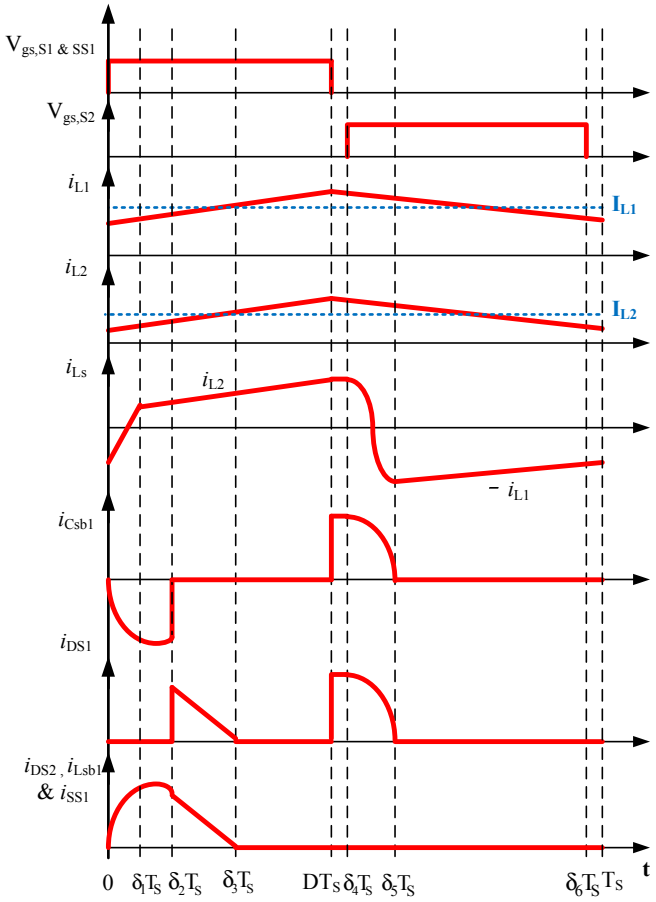


Figure 5. Major components current waveforms

1). *Switch RMS/Mean current calculation*

Based on earlier circuit operation analysis, when S_1 is on, I_{L1} will flow through S_1, I_{L2} will not go through S_1 until i_{Ls} changes polarity at $\delta_1 T_S$. Similarly, when S_2 is on, both I_{L1} and I_{L2} will flow through S_2 after until i_{Ls} changes polarity again at $\delta_5 T_S$. Then the two main switches' currents can be described as:

$$i_{S1} = \begin{cases} \frac{V_{Low}+V_H}{L_S} \cdot t, & 0 < t < \delta_1 T_S \\ I_{L1} + I_{L2}, & \delta_1 T_S < t < DT_S \\ 0, & DT_S < t < T_S \end{cases}, \text{ and} \quad (4)$$

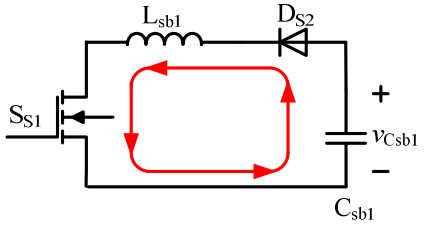
$$i_{S2}=\begin{cases}0 & ,\ 0<t<\delta_4 T_S\\ (I_{L1}+I_{L2})\cdot(1-\cos(\omega_1(t-\delta_4 T_S))), & \delta_4 T_S<t<\delta_5 T_S\\ I_{L1}+I_{L2} & ,\delta_5 T_S<t<DT_S\end{cases}. \quad (5)$$

where

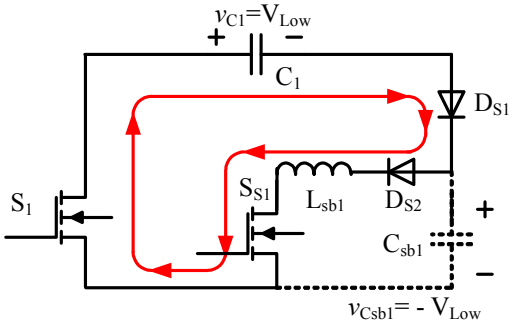
$\delta_1=\frac{L_S}{T_S}\cdot\frac{I_{L1}+I_{L2}}{V_{Low}+V_H}$, $\omega_1=\frac{1}{\sqrt{L_S\cdot C_{sb1}}}$, $\delta_4=(\frac{V_{Low}+V_H}{I_{L1}+I_{L2}})\cdot\frac{C_{sb1}}{T_S}+D$ and $\delta_5=\frac{\pi}{2\omega_1\cdot T_S}+\delta_4$.

Fig. 6 explains how the active snubber circuit realizes its functions during one switching period, the equivalent circuit between $\delta_3 T_S$ and DT_S is not shown since the active snubber circuit is not involved in any circuit operation. Again, for simplicity, the currents on L_1 and L_2 are assumed to be almost constant. When S_{S1} is turned on, the initial voltage on C_{sb1} can be written as:

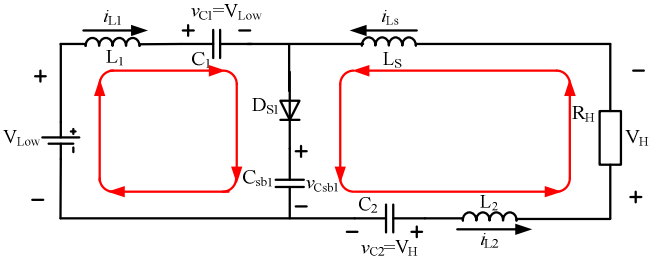
$$v_{Csb1\_initial}=V_H+(I_{L1}+I_{L2})\times\sqrt{\frac{L_S}{C_{sb1}}} \quad . \quad (6)$$



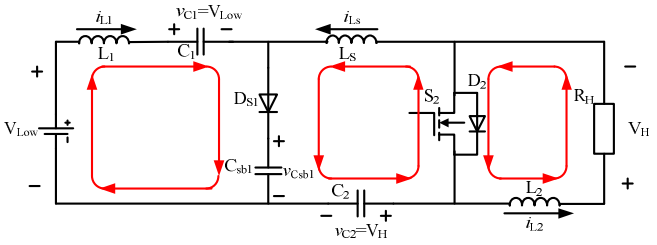
a) S_{S1} is on, from 0 to $\delta_2 T_S$.



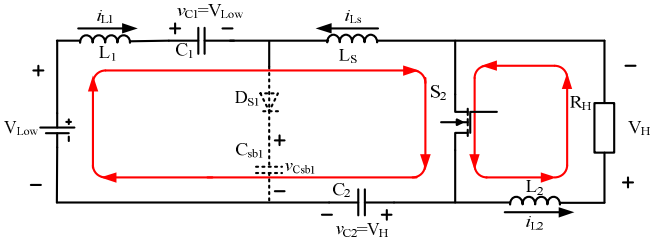
b) v_{Csb1} is clamped to $-V_{Low}$, from $\delta_2 T_S$ to $\delta_3 T_S$.



c) S_1 and S_{S1} are turned off, from DT_S to $\delta_4 T_S$.



d) S_2 is on, i_{Ls} decreases from I_{L2} to $-I_{L1}$, from $\delta_4 T_S$ to $\delta_5 T_S$.



e) $i_{Ls}=-I_{L1}$, from $\delta_5 T_S$ to T_S .

Figure 6. Active snubber circuit operation description

Since C_1 and C_2 are seen as voltage sources, the currents on switch S_{S1} and D_{S2} can be written as:

$$i_{SS1}=i_{DS2}=\begin{cases}\omega_2\cdot C_{sb1}\cdot v_{Csb1\_initial}\cdot\sin(\omega_2 t), & 0<t<\delta_2 T_S\\ (\omega_2\cdot C_{sb1}\cdot v_{csb1\_initial}\cdot\sin(\omega_2\delta_2 T_S))-\frac{V_{Low}}{L_{sb1}}(t-\delta_2 T_S), & \delta_2 T_S<t<\delta_3 T_S\\ 0, & \delta_3 T_S<t<T_S\end{cases}. \quad (7)$$

where

$\omega_2=\frac{1}{\sqrt{L_{sb1}\cdot C_{sb1}}}$, $\delta_2=(\arccos\frac{-V_{Low}}{v_{Csb1\_initial}})/(\omega_2 T_S)$, and

$\delta_3=\delta_2+(\frac{v_{Csb1\_initial}\cdot\sqrt{L_{sb1}\cdot C_{sb1}}}{V_{Low}\cdot T_S})\cdot\sin(\omega_2\delta_2 T_S)$.

Similarly the current on D_{S1} can be described as:

$$i_{DS1}=\begin{cases}0, & 0<t<\delta_2 T_S\\ (\omega_2\cdot C_{sb1}\cdot v_{Csb1\_initial}\cdot\sin(\omega_2\delta_2 T_S))-\frac{V_{Low}}{L_{sb1}}(t-\delta_2 T_S), & \delta_2 T_S<t<\delta_3 T_S\\ 0, & \delta_3 T_S<t<DT_S\\ I_{L1}+I_{L2}, & DT_S<t<\delta_4 T_S\\ (I_{L1}+I_{L2})\cos(\omega_1(t-\delta_4 T_S)), & \delta_4 T_S<t<\delta_5 T_S\\ 0, & \delta_5 T_S<t<T_S\end{cases}. \quad (8)$$

Then the RMS currents of the switches can be calculated based on following equation:

$$i_{SX\_RMS}=\sqrt{\frac{1}{T_S}\int_0^{T_S} i_{SX}(t)^2\,dt} \quad . \quad (9)$$

Also, the average currents of D_{S1} and D_{S2} can be obtained by using this equation:

$$i_{DSX\_Mean}=\frac{1}{T_S}\int_0^{T_S} i_{DSX}(t)dt \quad . \quad (10)$$

2). Capacitor RMS current calculation

The currents on two main circuit capacitors C_1 and C_2 can be described as:

$$i_{C1}=\begin{cases} I_{L1}-\dfrac{V_{Low}+V_H}{L_S}\cdot t, & 0<t<\delta_1 T_S \\ -I_{L2}, & \delta_1 T_S<t<DT_S \\ I_{L1}, & DT_S<t<T_S \end{cases}, \text{ and} \tag{11}$$

$$i_{C2}=\begin{cases} I_{L1}-\dfrac{V_{Low}+V_H}{L_S}\cdot t, & 0<t<\delta_1 T_S \\ -I_{L2}, & \delta_1 T_S<t<\delta_4 T_S \\ I_{L1}-(I_{L1}+I_{L2})\cdot\cos(\omega_1(t-\delta_4 T_S)), & \delta_4 T_S<t<\delta_5 T_S \\ I_{L1}, & \delta_5 T_S<t<T_S \end{cases}. \tag{12}$$

For C_{sb1}, the current can be written as:

$$i_{Csb1}=\begin{cases} -\omega_2\cdot C_{sb1}\cdot v_{Csb1\_initial}\cdot\sin(\omega_2 t), & 0<t<\delta_2 T_S \\ 0, & \delta_2 T_S<t<DT_S \\ I_{L1}+I_{L2}, & DT_S<t<\delta_4 T_S \\ (I_{L1}+I_{L2})\cos(\omega_1(t-\delta_4 T_S)), & \delta_4 T_S<t<\delta_5 T_S \\ 0, & \delta_5 T_S<t<T_S \end{cases}. \tag{13}$$

Similarly, the RMS current of every capacitor can be calculated as:

$$i_{CX\_RMS}=\sqrt{\frac{1}{T_S}\int_0^{T_S} i_{CX}(t)^2\,dt}\ . \tag{14}$$

3). Magnetic components RMS current calculation

Based on above analysis and calculation, the currents on magnetic components can be described as:

$$i_{Ls}=\begin{cases} -I_{L1}+\dfrac{V_{Low}+V_H}{L_S}\cdot t, & 0<t<\delta_1 T_S \\ I_{L2}, & \delta_1 T_S<t<\delta_4 T_S \\ -I_{L1}+(I_{L1}+I_{L2})\cdot\cos(\omega_1(t-\delta_4 T_S)), & \delta_4 T_S<t<\delta_5 T_S \\ -I_{L1}, & \delta_5 T_S<t<T_S \end{cases}, \tag{15}$$

$$i_{Lsb1}=i_{DS2}=\begin{cases} \omega_2\cdot C_{sb1}\cdot v_{Csb1\_initial}\cdot\sin(\omega_2 t), & 0<t<\delta_2 T_S \\ (\omega_2\cdot C_{sb1}\cdot v_{csb1\_initial}\cdot\sin(\omega_2\delta_1 T_S))-\dfrac{V_{Low}}{L_{sb1}}(t-\delta_1 T_S), & \delta_2 T_S<t<\delta_3 T_S \\ 0, & \delta_3 T_S<t<T_S \end{cases}. \tag{16}$$

For L_S and L_{sb1}, their RMS current can be calculated by using similar equation with (14); for L_1 and L_2, their RMS currents can be described as:

$$i_{L1\_RMS}=I_{L1}, \tag{17}$$

$$i_{L2\_RMS}=I_{L2}. \tag{18}$$

For transformer, it has both core loss and copper loss. The core loss calculation is similar to normal forward converter cases, thereby it is not elaborated here.

4). Influence of ac ripple current

For the two filter capacitors C_{Low} and C_H, only the ripple currents on L_1 and L_2 will flow through them and generate loss, the RMS value of the ac ripple currents can be calculated as:

$$i_{CLow\_RMS}=\frac{1}{2\sqrt{3}}\frac{V_{Low}\cdot D\cdot T_S}{L_1}, \text{ and} \tag{19}$$

$$i_{CH\_RMS}=\frac{1}{2\sqrt{3}}\frac{V_{Low}\cdot D\cdot T_S}{L_2}. \tag{20}$$

These ac ripple currents will also flow through other components, but their amplitude can be limited in a small range by selecting proper L_1 and L_2. Compared with the dc currents, the ac currents have small influence on the power loss of other components except C_{Low} and C_H, thereby the loss generated on other components by ac ripple currents can be ignored.

IV. SIMULATION AND EXPERIMENT RESULTS

A PSIM simulation model is built and the waveforms of proposed circuit are shown in Fig. 7 and Fig. 8, when V_{Low} = 8 V, I_{Low} = 50 A, and f = 100 kHz. In Fig. 7, switch S_{S1} and S_1 have the same gate signals. To show the soft switching and energy feedback functions clearly, the current waveforms are divided by a certain value to fit the corresponding voltage amplitudes. For example, Is1/10 is the current on S_1 divided by 10, ILsb1/5 is the current on L_{sb1} divided by 5 and Icsb1/10 is the current on L_{sb1} divided by 10. The ZVS off and ZCS on features of S1 are shown in the second window and the energy feedback function of Csb1 is verified by the third and forth windows. In Fig. 8, the time gaps between S_2 gate signal and switch voltage clearly show the soft switching of S_2 because of SR operation.

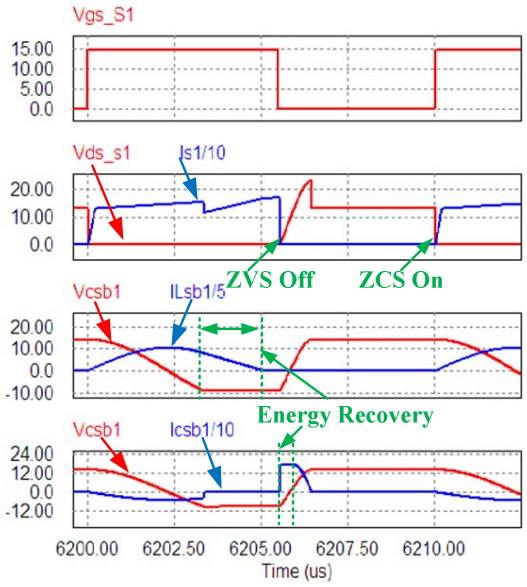


Figure 7. Low voltage side simulation results

A 1.2 kW prototype is shown in Fig. 9 and the experimental results which are carried out with the same parameters as simulation results are shown in Fig. 10 and Fig. 11. In these figures, v_{gs} is the MOSFET gate to source voltage, and v_{ds} is the MOSFET drain to source voltage. The ZVS off and the energy feedback functionalities of the active snubber circuit are illustrated in Fig. 10. Since there is no

current shunt connected with S_1, the ZCS on feature of S_1 is not shown in the experimental results.

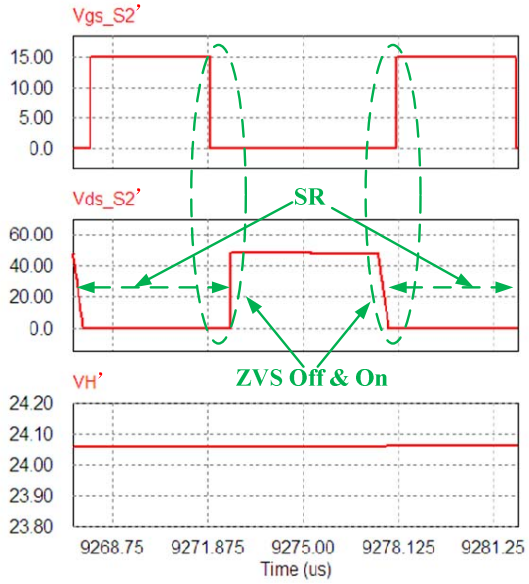


Figure 8. High voltage side simulation results

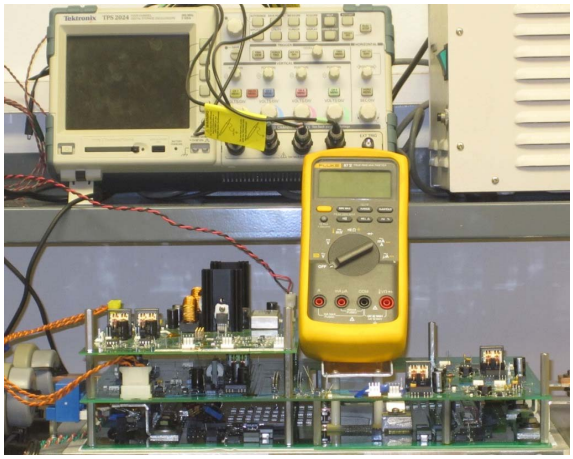


Figure 9. Prototype picture and test setup

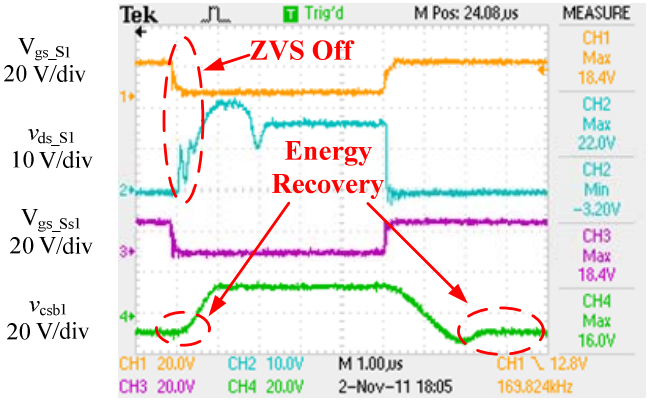


Figure 10. Low voltage side switching transients and snubber operation waveforms

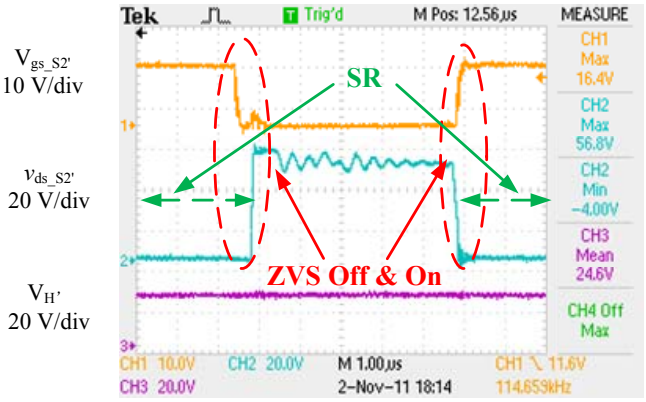


Figure 11. Zero voltage switching waveforms on high voltage side

Fig. 11 demonstrates the ZVS Off and On of S_2' because of the SR operation. For simplicity, the polarity of $v_{ds,S2'}$ is inverted to show a positive drain to source voltage under SR mode. When $v_{gs,S2'}$ reaches zero, $v_{ds,S2'}$ remains zero because D_2' is still conducting current. Similarly, because D_2' is forward biased before S_2' is turned on, $v_{ds,S2'}$ is already zero when $v_{gs,S2'}$ is rising.

Fig. 12 and Fig. 13 show the measured efficiency curves with Yokogawa WT – 3000 power analyzer.

The power loss calculation is carried out under V_{Low} = 6 V, I_{Low} = 200 A V_H' = 24 V, I_H' = 40.5 A, and the calculation results are shown in Table 2. All the resistance values are either given by datasheet or calculated according to the design parameters. For simplicity, all the values shown in Table 2 are low voltage side referred.

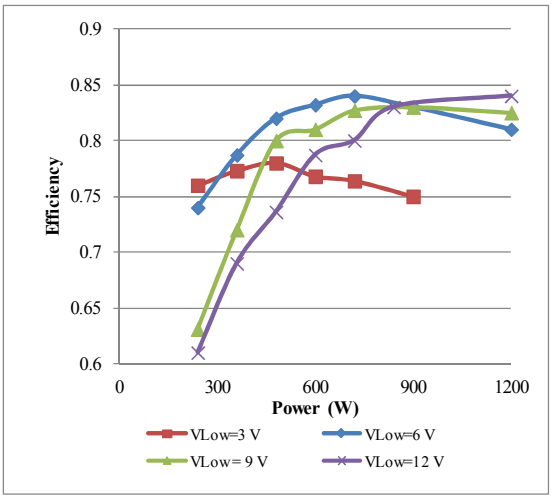


Figure 12. Efficiency curves

In the experimental results, when V_{Low} = 6 V and I_{Low} = 200 A, the efficiency is 81%, gives 228 W power loss, which is larger than the calculation result shown in Table 2. The contributing factors to this difference include cores' losses and resistive loss on PCB traces. The converter is built on a PCB with 4 oz/ft^2 copper layer. Nevertheless, when hundreds of amperes are flowing through the PCB board, there will be significant power loss. As a matter of fact, during the

experiments, in some places, the traces are hotter than the MOSFETs.

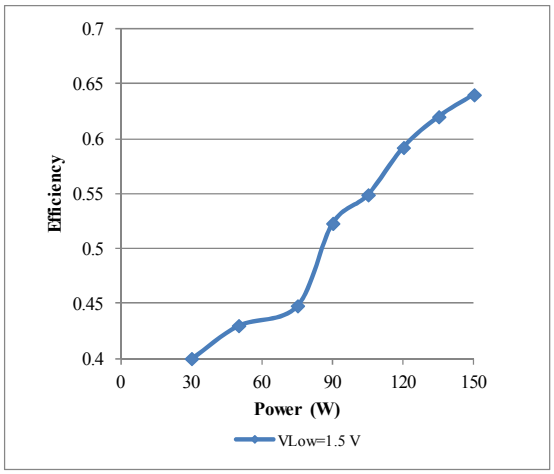


Figure 13. Efficiency curve when V_{Low} = 1.5 V

Also, the stray inductance in the circuit also makes some contribution to the total power loss. For example, in this prototype, the measured stray inductance near S_1 is 5 nH. When S_1 is switching off, the current flowing through this stray inductance is 320.5 A, thereby the energy stored in this stray inductance is 25.6 W at 100 kHz. In the current design, this power is dissipated through a RC snubber circuit and completely wasted.

TABLE 2 THE POWER LOSS CALCULATION AT V_{Low} = 6 V, I_{Low} = 200 A

Components	*Current (A)*	*Resistance (mΩ)*	*Power Loss (W)*
S_1	i_{S1_RMS} = 237.7 A	0.37	20.9
S_2	I_{s2_RMS} = 215 A	0.367	16.96
S_{S1}	I_{ss1_RMS} = 101 A	1.85	18.87
D_{S1}	i_{DS1_RMS} = 101 A $i_{DS\ 1\_Mean}$ = 50.6 A	V_{D0} = 0.4 V R_D = 1.25 mΩ	32.95
D_{S2}	$i_{DS\ 2\_RMS}$ = 101 A $i_{DS\ 2\_Mean}$ = 50.5 A	V_{D0} = 0.4 V R_D = 1.25 mΩ	32.95
C_1	i_{C1_RMS} =161.2 A	0.06	1.56
C_2	i_{C2_RMS} =156.2 A	0.017	0.41
C_{sb1}	i_{Csb1_RMS} =96.4 A	1.85	17.2
L_1	i_{L1_RMS} = 200 A	0.34	13.6
L_2	i_{L2_RMS} =121.5 A	0.18	2.66
L_{sb1}	i_{Lsb1_RMS} = 101 A	0.18	1.8
Transformer	i_{Tr_RMS} = 161.2 A	0.2	5.20
C_{Low}	i_{CLow_RMS} = 4.76 A	18	0.4
C_H	I_{ch_RMS} = 8.65 A	2	0.14
Total power loss			165.60 W

V. CONCLUSION

This paper presents bidirectional isolated dc/dc converter with wide input range and high boost ratio. The converter is designed as a universal interface between low voltage high current dc sources and 24 V dc systems. The circuit efficiency is improved by using a multifunctional active snubber circuit and energy recovery gate drive. This snubber circuit recovers the energy stored in the leakage inductance of the transformer, reduce the voltage overshoot on switching devices, and provide partial soft switching.

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