A voltage regulation method for high power switched-capacitor circuits

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Abstract—**This paper presented a voltage regulation method for high power switched-capacitor converters. The proposed method is based on a LC equivalent circuit of the capacitor charging loop, instead of the traditional RC equivalent circuit. The output voltage is regulated by varying the duration of the sinusoidal charging current. With the third quadrant operation of MOSFETs and optimized capacitor charging loop, the efficiency of the converter with the proposed voltage regulation method can exceed the theoretical maximum efficiency value for traditional methods. Detailed analysis and experimental results on a 200 W prototype is included in this paper.**

I. INTRODUCTION

The switched-capacitor circuit concept has been widely adopted in small-scale power conversions, with its advantage of light weight, low volume and high power density. The output voltage can be well regulated using various methods [1-5]. However, the traditional voltage regulation methods are based on a RC equivalent circuit of the capacitor charging loop, so the output voltage regulation mainly relies on the equivalent resistance in the circuit. As a result, the efficiency is low and a theoretical maximum efficiency exists [6-7]. For example, for a step-up switched-capacitor dc/dc converter with an ideal voltage transfer ratio of N, the maximum efficiency is $V_{out}/(N\times V_{in})$. This maximum efficiency largely limits the application of switched-capacitor converter in high-power voltage conversions, where high efficiency is required.

One important difference between low-power and high-power switched-capacitor converters is the impedance of the capacitor charging loop. The RC equivalent circuit is only accurate in describing resistor-dominant charging-loop impedance. But for most high-power converters, which have low resistance and large inductance in the charging loop, an LRC or LC equivalent circuit is more accurate. The LC equivalent circuit has been utilized in [8-10], where the loop inductance is utilized to oscillate with the dc capacitors to realize soft-switching. In this paper, the LC equivalent circuit is adopted to present a voltage regulation method. In the proposed method, the angle of the sinusoidal charging current is adjusted, so the output voltage regulation can be realized.

To achieve minimum power loss and reduce EMI noises, the switching devices (MOSFETs) are working in the third quadrant. In this way, when the charging process stops, the remaining current of the stray inductance can free-wheel in the circuit. Therefore, the remaining energy in the stray inductors is absorbed by the capacitors, rather than wasted. As a result, a high efficiency voltage regulation can be achieved.

The rest of this paper is organized as follows: in Section II, a detailed analysis on the shape of capacitor charging current is presented. Based on this analysis, the proposed voltage regulation method is introduced in Section III. Practical design concerns, including the third quadrant operation and peak current reduction, are discussed in Section IV. Finally, the experimental results on a 200 W switched-capacitor voltage doubler are presented in Section V.

II. AN ANALYSIS ON THE CAPACITOR CHARGING CURRENT

A simple circuit to analyze the charging current of a switched-capacitor converter is the series RLC circuit shown in Fig. 1 (a). In this circuit, the switch S is closed at t=0. The voltage source ΔV represents the voltage difference between the voltage sources and the capacitor being charged. The stray inductance and resistance of this current charging loop are lumped together as Ls and Rs. For this RLC circuit, the damping factor ς is defined as:

$$\varsigma = \frac{R_s}{2}\sqrt{\frac{C}{L_s}}. \quad (1)$$

The damping factor determines the shape of the charging current. Fig. 1 (b) shows the shape of the charging current at three different damping factors of a switched-capacitor circuit. It can be seen in Fig. 1(b) that with a damping factor of 0.1, the charging current has no oscillation and can be regarded as a square waveform. While with a damping factor of 10, the shape of the charging current is almost sinusoidal.

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For switched-capacitor converters with small power ratings, especially small current ratings, they are more likely to have a large damping factor. This is due to the fact that the small size of components results in a large loop resistance, which becomes the dominant factor in the loop impedance. While for converters with large current ratings, it is required for both capacitors to have low ESR and switches to have low on-resistance to guarantee the efficiency. In this case, the loop resistance may not dominate the impedance equation and the damping factor can be much smaller than 1, which will result in a sinusoidal charging current shape.

In the following analysis, the damping factor is assumed to be much smaller than 1, so the current has a sinusoidal shape, and the capacitor charging loop can be represented by a simple LC circuit.

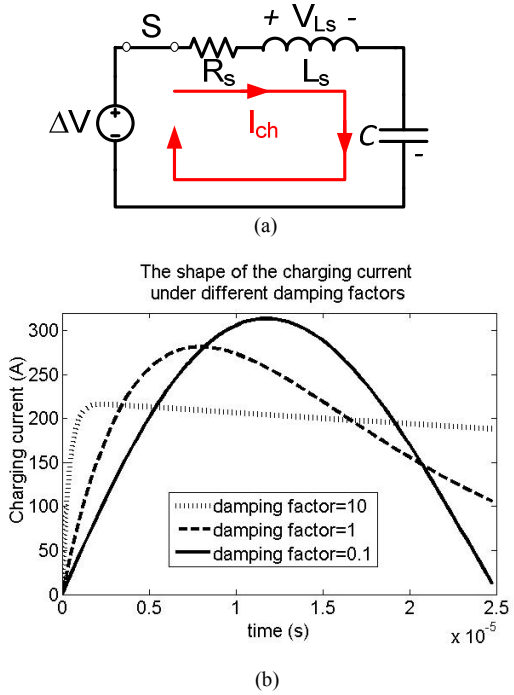


Fig.1. (a) The RLC equivalent circuit for the current charging loop. (b) The shape of the charging current with different damping factors.

III. THE OUTPUT VOLTAGE REGULATION METHOD

The charging process for a capacitor in a switched-capacitor circuit can be analyzed using the circuit shown in Fig.2. In this simple circuit, there are two operation modes, which are shown in Fig.2 (a) and (b), respectively. The duration of the first mode is assumed to be D×T, where D is the duty ratio of S_1 and T is the switching cycle.

In the first operation mode, the two switches S_1 and S_2 are turned on and the voltage source V_{in} charges the capacitor with a sinusoidal-shape current. The peak of capacitor charging current is assumed to be I_{peak}, and the frequency is decided by the stray inductance L_S and the capacitance of the capacitor C. The capacitor current $i_C(t)$ in this interval can be expressed as:

$$i_C(t) = \mathrm{I}_{peak}\sin(\omega t), 0 < t < DT \tag{2}$$

where ω is the oscillation frequency of the sinusoidal charging current. In the second interval, S_1 and S_2 are turned off and the capacitor discharges to the load with a constant current. Assume the load current is I_d, then the amount of charge needs to be sent to the load is $T \times I_d$. Based on the charge balance on the capacitor:

$$D\frac{T}{\theta_0}\int_0^{\theta_0}(\mathrm{I}_{peak}\sin(\omega t))d\theta = T \times I_d, \tag{3}$$

where θ_0 is the angle of the sinusoidal charging current when the switches are turned off, and $\theta_0 = D\omega T$.

Solving (3), the amplitude of the charging current can be calculated as:

$$I_{peak} = I_d\theta_0 / D(1-\cos\theta_0). \tag{4}$$

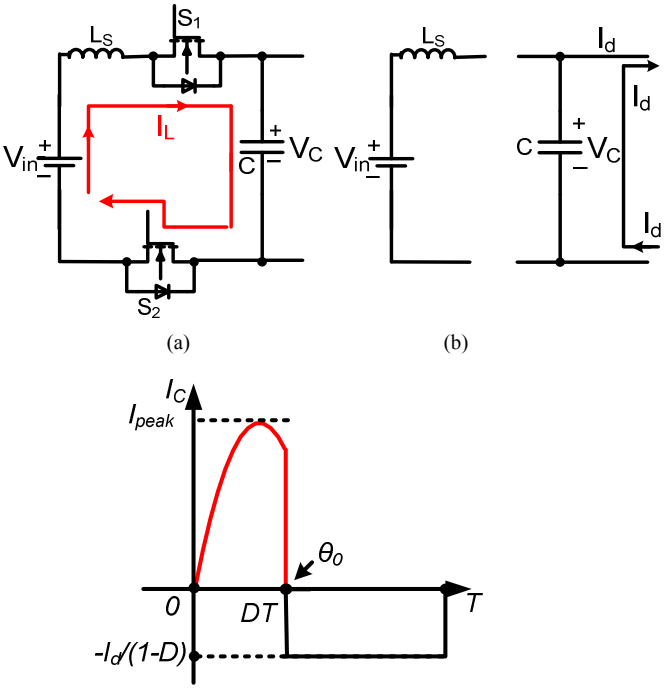


Fig.2. The equivalent circuit of a simplified switched-capacitor circuit. (a).Operation mode I. (b). Operation mode II. (c). The waveform of the capacitor current.

The voltage of the capacitor during the charging process can be expressed as:

$$V_C(t) = V_{C0} + \frac{1}{C}\int_0^t(I_{peak}\sin(\omega t))d\tau = V_{C0} + \frac{1}{C}[\frac{I_{peak}}{\omega}(1-\cos(\omega t))], \tag{5}$$

where V_{C0} is the initial voltage of the charging process. V_{C0} is also the minimum capacitor voltage.

The maximum voltage occurs at t=DT, which can be calculated as:

$$V_{C\_\max} = V_C(DT) = V_{C0} + Ti_d / C. \tag{6}$$

The relationship between the dc input voltage and the instantaneous value of output voltage can be expressed as:

$$V_{in} = L_S \frac{di_{Ls}}{dt} + V_{out}(t) = L_S I_{peak} \omega \cos(\omega t) + V_{out}(t). \quad (7)$$

At t=DT, $V_{out}(DT) = V_{C\_\max}$, thus V_{C0} can be calculated as:

$$V_{C0} = V_{in} - L_S I_{peak} \omega \cos(\theta_0) - T i_d / C. \quad (8)$$

Because $\omega = 1/\sqrt{L_S C}$,

$$\begin{aligned} L_S I_{peak} \omega \cos(\theta_0) &= L_S I_d DT \omega^2 \cos(\theta_0) \\ &= I_d T \cos(\theta_0) / C(1 - \cos\theta_0), \end{aligned} \quad (9)$$

thus:

$$V_{C0} = V_{in} - T i_d / C(1 - \cos\theta_0). \quad (10)$$

During the capacitor charging period, the average voltage is:

$$\begin{aligned} V_{C\_avg\_ch} &= V_{C0} + \frac{1}{CDT}\int_0^{DT} [\frac{I_{peak}}{\omega}(1 - \cos(\omega t))]dt \\ &= V_{C0} + \frac{T}{C} i_d \frac{1 - \frac{\sin\theta_0}{\theta_0}}{(1 - \cos\theta_0)}. \end{aligned} \quad (11)$$

During the capacitor discharging period, the average voltage is:

$$V_{C\_avg\_dis} = (V_{C0} + V_{C\_\max})/2 = V_{C0} + T i_d / 2C. \quad (12)$$

The average capacitor voltage can be calculated as:

$$\begin{aligned} V_{C\_avg} &= D V_{C\_avg\_ch} + (1 - D) V_{C\_avg\_dis} = \\ & V_{in} - \frac{T}{C} i_d [\frac{1 - D(1 - \frac{\sin\theta_0}{\theta_0})}{(1 - \cos\theta_0)} - \frac{1 - D}{2}]. \end{aligned} \quad (13)$$

Because $\theta_0 = D\omega T$, (13) suggests that, if the switching frequency and capacitance are constant, the capacitor voltage depends on the termination angle of the charging current and the value of the load current. As a special case, if D=1/2 and $\theta_0 = 180°$, which is the condition for the soft-switching scheme in [8], the average capacitor voltage equals the input voltage.

The duration (or the termination angle) of the sinusoidal capacitor charging current can be adjusted to realize the output voltage regulation. To accurately control the output voltage, the output current can be measured and used as one feedback variable.

Figure 3 plots the output voltage at different charging current termination angles for a converter which has an input voltage of 50 V, a switching frequency of 50 kHz and load current of 10 A. The capacitance is assumed to be 50 μF and the duty ratio is assumed to be 0.5. It can be seen that the output voltage drops exponentially as θ decreases. When the capacitor charging angle is higher than 90º, the voltage regulation only has a range of around 2.5 V. While when the angle is reduced to 50 º, the output voltage range is 10V. This figure shows that, the lower the capacitor charging angle, the higher the voltage regulation capability.

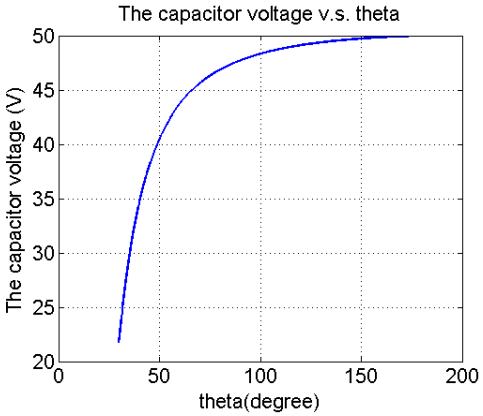


Fig.3. The capacitor voltage v.s. θ_0 for the a converter with 50 V input voltage.

Since no resistive components are used in this voltage regulation method, the efficiency is not proportional to the output voltage. As a result, the traditional upper limit on the efficiency does not exist for the proposed method.

However, this voltage regulation method does affect the efficiency of the converter in other aspects. Firstly, since switches are turned off at non-zero conditions, the soft-switching scheme proposed in [8] cannot be used, which adds the switching loss. Also, the voltage regulation is achieved by changing the angle of the capacitor charging current, a large peak charging current and large conduction loss may be resulted from a reduced charging current angle.

The aforementioned analysis is for capacitors that are not used as output capacitors. Same analysis method can be used to analyze the case when the capacitor is used as an output capacitor, which yields similar results.

IV. PRACTICAL DESIGN CONSIDERATION

The last section gives a general method on how to regulate the output voltage by controlling the angle of the charging current. However, when comes to the practical design, there are several problems that have to be solved before the converter can be realized. Two main problems and their solution are discussed in the paper.

A. The residue current in the stray inductance—the third quadrant operation of MOSFETs

Since the switches are turned off at non-zero conditions, the residual current in the stray inductance has to find a path to flow, otherwise this energy stored in the stray inductance will be wasted as power loss, and huge EMI noises will be generated due to the large di/dt.

To solve this problem, if MOSFETs are used as the switching devices, they need to work in the third quadrant, which means the current flows from the source to the drain of the MOSFET. In that way, the parallel diode will immediately pick up the remaining current after the MOSFET are turned

off, so the current in the stray inductance can continue to flow. Residue current free-wheeling loop has to be carefully designed so that the current can be reduced to zero in a reasonable time to reduce the EMI problem.

Fig.4 shows a voltage doubler circuit with variable output voltage capability. In this voltage doubler, MOSFETs S_1 and S_4 work in the third quadrant, while S_2 and S_3 operate in the first quadrant. The PCB layout of the voltage doubler is specially designed so most stray inductance is near the two third-quadrant-operated switches S_1 and S_3. The output voltage regulation is achieved by varying the angle of the charging current in the upper stage. The lower stage operates with 180 degree charging current, so soft-switching can be achieved for the lower stage.

The remaining current after switches are turned off can be calculated using:

$$I_{LS} = \frac{I_d \theta_0}{D} \frac{\sin\theta_0}{1-\cos\theta_0}. \quad (14)$$

When S_1 is turned off, the remaining current in the leakage inductance flows through its body diode. One possible current flowing path is shown in Fig. 4. Since there is much less stray inductance associated with S_3 than S_4, most remaining current of L_S flows through C_1 and S_3, and then back to S_1. The time needed for the free-wheeling current reduces to zero is:

$$t_{fw} = \frac{L_s \times I_{LS}}{V_C}. \quad (15)$$

The energy from the stray inductance will be absorbed by C_1, the voltage rise ΔV_C can be calculated from (16):

$$\frac{1}{2} L_S I_{LS}^2 = \frac{1}{2} C[(V_C + \Delta V_C)^2 - V_C^2]. \quad (16)$$

Solving (16), $\Delta V_C \approx \frac{1}{2} \frac{L_S I_{LS}^2}{C V_C}$.

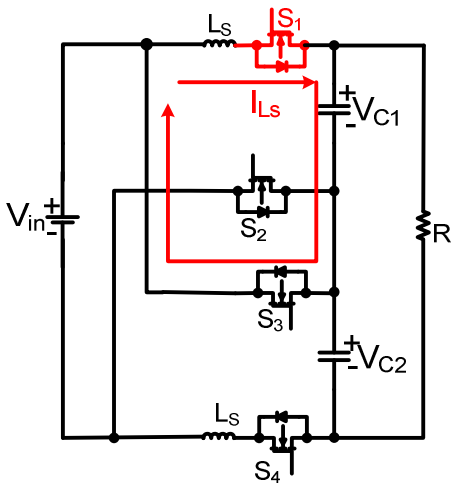


Fig.4. A voltage doubler with variable output capability.

B. *The peak current reduction*

When the switching angle is adjusted to regulate the output voltage, the capacitor charging time also changes. A reduction of the charging time results in a larger current peak value of the switches. For example, for the voltage doubler shown in Fig.4, the duty ratio for both stages is 0.5 and the charging current angle is 180° under normal soft-switching operation condition. Therefore, the total charge is delivered to the load in a total time of T/2. If the charging current angle of the top stage is changed to 90°, then the same amount of electric charge needs to be delivered to the load in T/4, which results in a peak charging current around two times the value in the first case.

As a result of the reduced charging time, both the peak current and conduction losses of MOSFETs are increased. Therefore, the regulation capability of the proposed method is limited by the maximum safe peak current of the MOSFETs, which is determined by the minimum charging current angle.

From Fig. 3, it can be seen that the voltage regulation capability increases exponentially with the reduction of the termination angle of the charging current. For $\theta_0 \geq 90°$, the voltage regulation range is very small. To achieve a good voltage regulation range while avoiding a large peak current, it would be beneficial for the top stage of the voltage doubler to have a smaller oscillation frequency than the lower stage. For example, if the top stage has an oscillation frequency one half of the lower stage and the lower stage has a charging current angle of 180° to realize soft-switching, then maximum charging current angle of the top stage is 90°. Compared to the normal case where both stages have the same oscillation frequency, a smaller reduction on the capacitor charging time is needed to achieve the same voltage regulation. As a result, the peak current can be reduced.

V. EXPRIMENTAL RESULTS

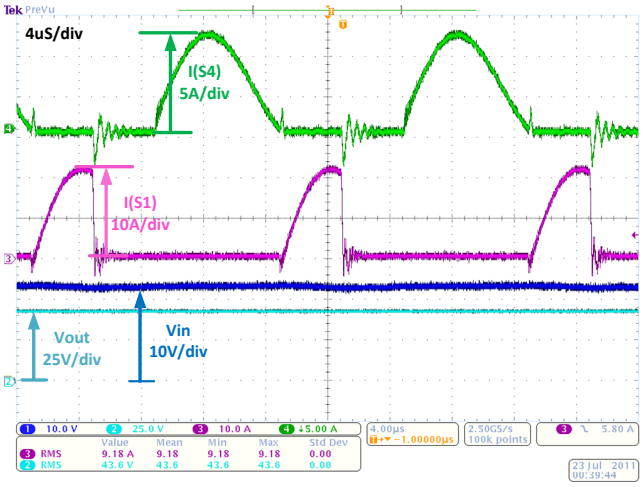
A voltage doubler has been built using two switched-capacitor prototype boards. The switching device used in this prototype board is IRFI4410ZPbF MOSFET. Ten C5750X7R2A475K ceramic capacitors with a voltage rating of 100 V and a capacitance of 4.7 uF are put in parallel as one main capacitor. The equivalent resistance and inductance of the capacitor charging loop is 15 mΩ and 118 nH, respectively. The damping factor at this test condition is around 0.15.

An efficiency test has been performed to prove the method proposed in this paper. The input power of this test is fixed at 200 W. The switching frequency is around 40 kHz and the input voltage is 20 V.

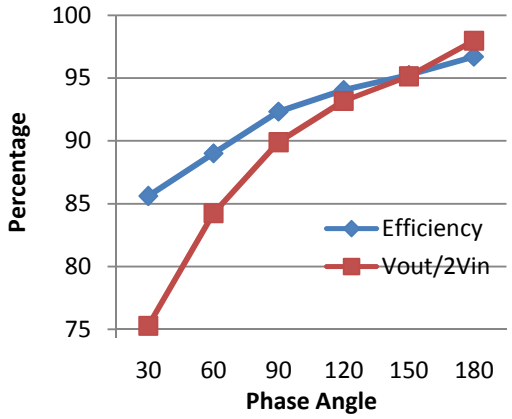
Fig.5 (a) shows the charging current waveform of the lower stage (the top trace), which has an angle of 180º, and the upper stage (the second trace from the top), which has an angle of 100º. It can be seen that soft-switching is achieved for the lower stage. The average input voltage is 24.0 V and the average output voltage is 43.6 V, showing that the output voltage is 91% of the voltage.

The efficiency of this voltage doubler is measured with a Yokogawa WT3000 power meter and LEM IT 700-S high

performance current transducer. The efficiency and voltage regulation ratio (Vout/2Vin) of the converter is plotted together in Fig.5 (b). For most points on the curve, the efficiency is higher than $V_{out}/2V_{in}$, which is the theoretical highest efficiency with traditional methods. The only exception is for the last points, where the efficiency is limited by the basic converter conduction and switching loss. This proves that the proposed method can achieve higher efficiency than previous methods where the highest efficiency is the voltage regulation ratio ($V_{out}/2V_{in}$ in this case).



(a)



(b)

Fig.5. The experimental results on a voltage doubler. (a) The input/output voltage and switch current waveforms. (b) The efficiency curve and voltage ratio curve.

It should be noticed that since the tested prototype boards have not been optimized according to Section IV, the efficiency number is still low. For example, both S_1 and S_2 have similar stray inductance, so half of the energy in the stray inductance cannot be sent back to the capacitor and is wasted. S_2 experiences a large di/dt when it is turned off. It can also be seen that the peak current of the S_1 is much larger than the peak current of S_4 in the lower stage, since both stages have the same loop stray inductance. By employing the methods provided in Section IV, a higher efficiency curve can be achieved.

VI. Conclusions

A voltage regulation method for high power switched-capacitor converters is presented in this paper. The proposed method adopts a LC equivalent circuit of the capacitor charging loop. The output voltage regulation is achieved by varying the switching angle of the sinusoidal charging current. To reduce the power loss and EMI noises, the third quadrant operation of MOSFETs and special stray inductance arrangement need to be utilized. Basic theoretical analysis and initial experimental results from a switched-capacitor testing board are included in the paper. More detailed analysis and the experimental results on a new board with optimized stray inductance distribution will be included in the follow-up papers.

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