# Minimum Power Loss Control – Thermoelectric Technology in Power Electronics Cooling

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***Abstract* -- This paper investigates the possibility of using thermoelectric cooling (TEC) modules to improve the power density of power electronics systems. A simple test setup served for comparison purposes is built. The result shows that, through the use of TEC modules to actively cool power electronics devices, the power handling capability is improved versus that of an identical passively cooled system. Then a minimum power loss control strategy for TEC is proposed. Experimental results are shown to demonstrate the effectiveness of the proposed control strategy.**

***Index Terms*-- Active Cooling, Minimum Power Loss, Power Electronics, TEC, Thermoelectric Technology, Thermoelectric Cooling.**

## I. Nomenclature

| *Symbol* | *Quantity* | *Units* |
|---|---|---|
| $I_D$ | MOSFET drain current | Amps (A) |
| $R_{DS_on}$ | MOSFET on-state resistance | Ohms (Ω) |
| $T_{amb}$ | Ambient temperature | K |
| $I_{TEC}$ | Current delivered to the TEC module | Amps (A) |
| $T_{hot}$ | Hot side TEC module temperature from datasheet | K |
| $I_{max}$ | Maximum TEC module current | Amps (A) |
| $V_{max}$ | Maximum TEC module voltage | Volts (V) |
| $\Delta T_{max}$ | Maximum TEC module temperature difference | K |
| $\alpha_{TEC}$ | Seebeck coefficient of the TEC module | V/K |
| $R_{TEC}$ | Electrical resistance of the TEC module | Ohms (Ω) |
| $R_{th_TEC}$ | TEC module thermal resistance | K/W |
| $R_{th_TEC_app}$ | Apparent TEC module thermal resistance, function of $I_{TEC}$ | K/W |
| $\Delta T_{TEC_app}$ | Apparent temperature pump of the TEC module, function of $I_{TEC}$ | K |
| $\Delta T_{ca}$ | Temperature difference between TEC module cold side and ambient air | K |
| Q | MOSFET power loss | Watts (W) |
| $R_{th_al}$ | Thermal resistance of the aluminum heat spreader | K/W |
| $T_j$ | MOSFET junction temperature | K |

## II. Introduction

Due to the limitations on weight, cost and packaging space, high power density is always desired in power electronics applications. To improve the power density, integrated design approaches are needed which include design considerations not only on power electronics, but also on the cooling system.

Traditional cooling methods, including forced air or water cooled heatsinks [1], [2], refrigerant based cooling [3], [4], and synthetic jets [5], have been extensively studied to increase the heat dissipation capability of the power electronics systems. But in real applications, most of these methods suffer from different problems including increased components size and weight, slow response time and large acoustic noises. With these cooling methods, it is hard to have an integrated and effective control of both power electronics circuits and their cooling units.

Recent advances in the design of TEC modules have made it suitable for a wide range of applications. For chip designs, Yang B. et al presented a "mini-contact" method for on-chip hot-spot cooling which can make the cooling 19°C better than conventional methods [6]. In telecom applications, the TEC is used to cool the laser diode in a pump laser chip package for optical transmission system [7]. In CPU cooling, liquid cooling systems with TEC can significantly increase its thermal performance [8]. However, the application of TEC in cooling power electronics devices has not been sufficiently studied.

This paper studies the pros and cons of utilizing thermoelectric cooling (TEC) modules to improve the power density of power converters. Then based on the observations from a comparison test, a minimum power loss control strategy is proposed.

The work documented in this paper indeed is just the first part of a series of efforts in utilizing TEC modules in power electronics circuits. The ultimate goal is to demonstrate a system that uses a single micro-controller to control both the main power stage and the TEC unit, thus to realize integrated control of both power electronics circuits and their active cooling units, which in turn would result in best power density. The proposed system in the vehicular application condition is shown in Fig.1.

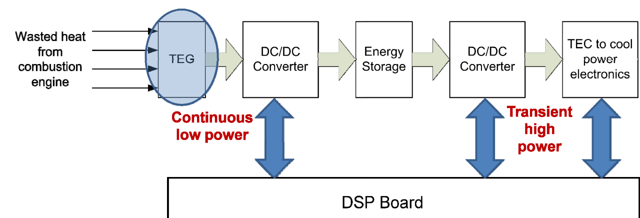


Fig. 1. The proposed power/cooling integrated control system

For the above system, in normal operating conditions the wasted heat from an engine is absorbed by a thermoelectric generation (TEG) module and stored in energy storage devices such as a battery through a dc/dc converter. When

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transient high power is needed, the DSP will control the TEC and its front end converter to cool the power electronics circuit with the power provided by the battery and the TEG. This closed and integrated control scheme will ensure the system operates at an optimized cooling condition and thus the power density of the whole system could be improved. The minimum power loss control strategy proposed in this paper is the enabling technology and the back bone of the envisioned system.

## III. A Comparative Test for Passive Cooling and TEC Based Cooling in Power Electronics Systems

As the first step, a comparative test between passive cooling and TEC based cooling is performed to investigate the pros and cons of using TEC in the power electronics cooling. The power electronics circuit diagram is shown in Fig. 2. An Infineon SPW35N60CFD power MOSFET is employed as the power electronics device. This MOSFET's gate is connected to a 12V dc source through a current limiting resistor forcing it to be closed at all time. Under this circumstance, the only power loss of the MOSFET is its on-state loss and the only parameter of interest is its on-state resistance. The adjustable resistor $R_{load}$ is used to adjust the MOSFET drain current $I_D$.

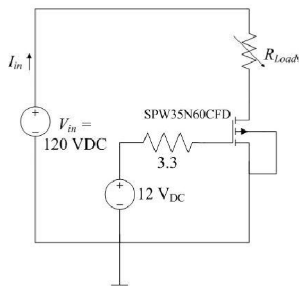


Fig. 2. Schematic diagram of the power electronics test circuit.

To examine the TEC based active cooling, the TEC cooling apparatus is built, as shown in Fig.3. The MOSFET on the top works as a heat source. An aluminum plate is placed between the MOSFET and the TEC module serving as a heat spreader to increase the contact surface area between the MOSFET and the TEC. A heat sink and a 12V fan are placed below the TEC module to dissipate the heat on its hot side.

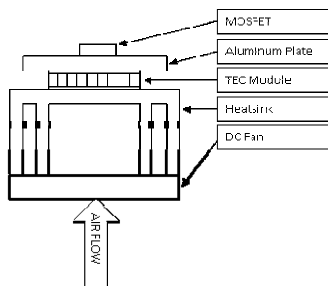


Fig. 3. The structure of TEC cooling apparatus.

An identical test apparatus to that of Fig. 3, omitting the TEC module and the aluminum heat spreader, is constructed to mimic the passive cooling condition. The whole test setup is shown in Fig. 4.

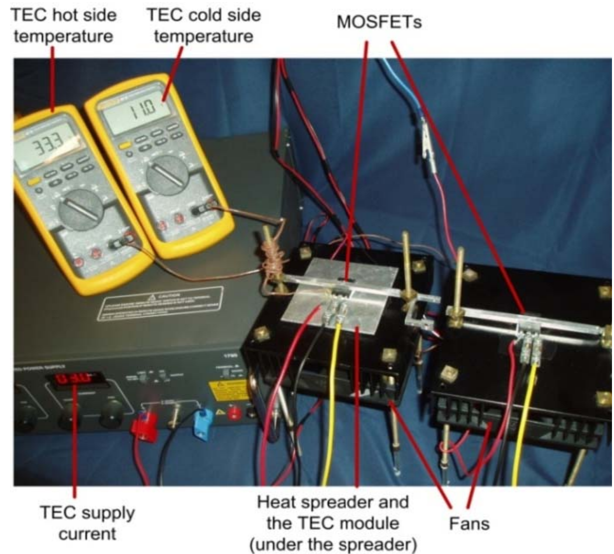


Fig. 4. The experimental setup for the comparative test.

Firstly, the MOSFET power losses at different drain currents are tested. The TEC current $I_{TEC}$ is set to be 3 A in this test. Fig. 5 shows the difference in MOSFET power loss between active cooling and passive cooling. It can be seen that, at low $I_D$, the two methods have similar power losses. But at high $I_D$ values (larger than 21 A), the TEC based cooling results in less power loss, which is due to a lower on-state resistance of MOSFET.

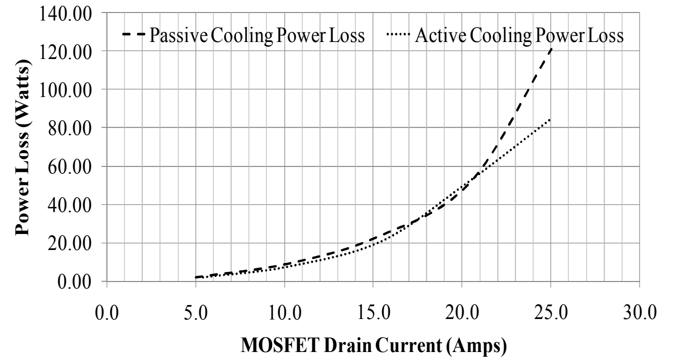


Fig. 5. Experimental power loss comparison.

Fig. 6 shows the power spent to drive the TEC module along with the power loss saved in the MOSFET when comparing the active cooling and the passive cooling methods. Again, Fig. 6 confirms that there is minimal benefit for using the TEC module when the drain current is less than 21 A, but when the MOSFET drain current exceeds 21 A the benefits of active cooling becomes apparent. The extra benefit is seen after the MOSFET drain current reaches

24 A at which point the saved power loss is higher than the power fed to the TEC module. This implies the total system power is saved after using the TEC module. Although this paper does not focus on the system total power, this result opens doors for further studies. Also please note that in this test the TEC current is not optimized.

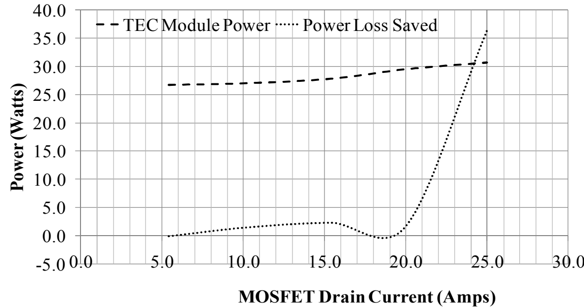


Fig. 6. Power loss savings and the driven power of TEC.

Then, focusing only on the MOSFET power loss, a sweeping TEC current test is conducted to gather a family of curves corresponding to different drain currents through the MOSFET, which is shown in Fig. 7. It is clear to see the parabolic nature of power loss in the 20 A drain current curve. The minimum power loss is at approximately 5.5 A TEC current. If a TEC is powered with a current lower than 5.5A, there is not sufficient heat pumping and the MOSFET power loss increases. If the TEC is over-driven above 5.5 A, the MOSFET power loss also increases because the internal heat generated by the TEC module causes the system temperature to rise. The bottom three lines are also parabolic, although the vertical scale doesn't support this visually. The parabolic shape of MOSFET power loss indicates a minimum power loss point could be found, and this is the foundation of the proposed minimum power loss algorithm.

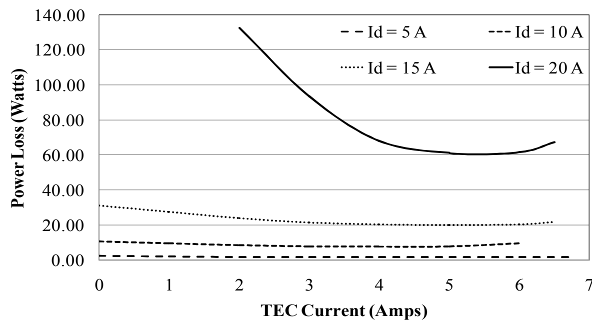


Fig. 7. Power loss vs. sweeping TEC current.

## IV. The Problems of the TEC based Active Cooling

Though it is clear that the TEC based cooling does have the capability to lower the MOSFET power loss, the experimental results revealed some negative aspects of the TEC based active cooling method:

### *A. Additional energy spent to drive the TEC module*

The TEC module needs a driven current, which introduces additional energy to the whole system. From Fig. 6, with low MOSFET drain current, the energy spent to drive the TEC is much greater than the power loss saved. So, it is not economical to operate a TEC module in low power conditions. However, starting from a point (~24A), the power loss saved in the MOSFET exceeds that spent to drive the TEC module. This is the extra benefit TEC offers.

### *B. Thermal Resistance of the TEC Module*

As seen in the experimental setup, the TEC module adds an additional layer of material that impedes thermal transfer from the heat source to the heatsink. An unpowered TEC module has an inherent thermal resistance that can be calculated from ratings provided on the manufacturer's datasheet [9]. But the experiment results also show that despite the additional thermal resistance introduced by the TEC module and the silicon grease layers on both sides of the module, there is little to no degradation of the cooling system when the power electronics devices are operated in low power ranges. This is shown in the experimental data presented in Fig. 8.

The results from curves in Fig. 8 show that there is little to no degradation of the cooling performance if TEC is not operating at low power range. Thus, to save energy, in this test setup, the TEC module can be commanded to operate only when the power electronics load exceeds a certain threshold.

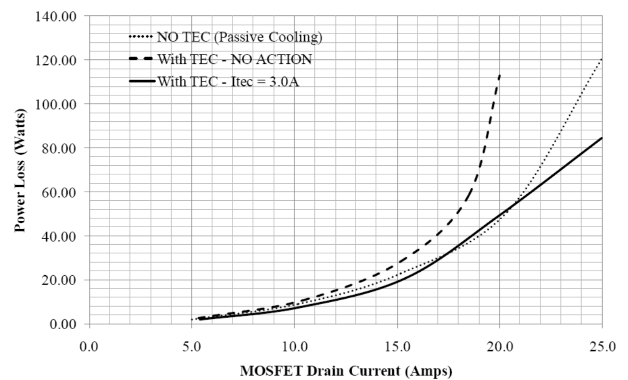


Fig. 8. MOSFET power loss comparison with added thermal resistance of unpowered TEC module.

### *C. Additional Heat Introduced by an Over-Driven TEC Module*

Since the TEC module is also producing power loss, the system temperature will increases if excessive current is pumped into the TEC module. This together with the results of Fig. 6 shows that finding a minimum power loss point for the TEC application is possible. This phenomenon is easy to visualize in Fig. 7 where all power loss curves are parabolic. A minimum power loss is thus achievable and it corresponds to a specific TEC current. This is the basis of

the proposed minimum power loss control algorithm.

## V. Proposed Minimum Power Loss Control

Based on the results presented so far, an energy saving does exist at high load conditions. Also, based on the parabolic nature of power loss curves, an optimal TEC operating point can be identified and achieved. The proposed minimum power loss control system is presented in Fig. 9. It consists of four parts: the TEC model, the power electronics model, the minimum power loss controller and the dc/dc converter.

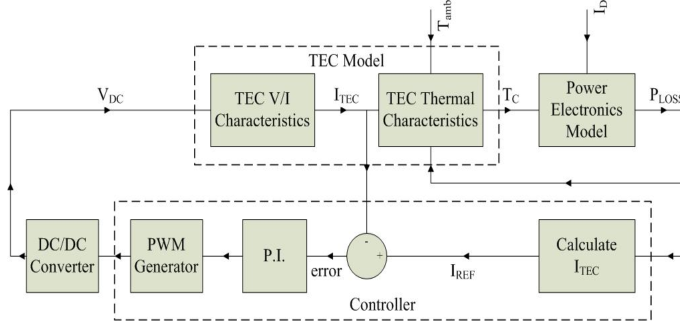


Fig. 9. Proposed minimum power loss control system.

### A. TEC Model

The TEC model calculates the cold side temperature of the TEC module using only data in the datasheet for the TEC module and the heatsink, along with TEC current, ambient temperature, and instantaneous power loss [10], [11]. The Seebeck coefficient, the electrical resistance, and the thermal resistance of the TEC module are calculated using (1), (2), (3), respectively.

$$\alpha_{TEC} = \frac{V_{\max}}{T_{hot}} \quad (1)$$

$$R_{TEC} = \frac{V_{\max}}{I_{\max}} \times [\frac{T_{hot} - \Delta T_{\max}}{T_{hot}}] \quad (2)$$

$$R_{th_TEC} = \frac{\Delta T_{\max}}{I_{\max} V_{\max}} \times [\frac{2T_{hot}}{T_{hot} - \Delta T_{\max}}] \quad (3)$$

The temperature difference between the TEC cold side and ambient temperature is calculated using (4)

$$\Delta T_{ca} = QR_{th_TEC_app} + \Delta T_{TEC_app} \quad (4)$$

$\Delta T_{ca}$ is a function of TEC current, and takes into account the temperature across the specific heatsink/fan used in this experiment. Simply adding ambient temperature to the result of (4) gives the cold side temperature of the TEC module. This temperature will be adjusted as in (5) to account for the thermal resistance of the aluminum heat spreader. The result essentially is the MOSFET case temperature.

$$T_C = \Delta T_{ca} + T_{amb} + QR_{th_al} \quad (5)$$

### B. Power Electronics Model

This model calculates the power loss of the MOSFET. $T_C$ is adjusted by adding $Q \times R_{th_jc}$ to give $T_j$. The MOSFET on-state resistance can be calculated with (6), which is derived from information provided in the datasheet:

$$R_{DS_on}(T_j) = 3.114\times10^{-6} T_j^2 + 0.6396\times10^{-3} T_j + 0.09972 \quad (6)$$

To calculate the power loss in the MOSFET, the on-state resistance with the external input of drain current $I_D$ will be used as in (7).

$$P_{loss} = I_D^2 \times R_{DS_on}(T_j) \quad (7)$$

The result of (7) gives the estimated power loss based on the TEC current command from the controller, the ambient air temperature, and the drain current through the MOSFET. This quantity is an input to the controller and is the quantity of interest to be minimized.

### C. Controller

The controller is developed and simulated using Matlab/Simulink. To ensure the system operates at the minimum portion of the curve shown in Fig. 7, the derivative of $P_{loss}$ is forced as close to zero as possible. When power loss exceeds the preset threshold, the controller will calculate the TEC reference current and turn on the dc/dc converter which drives the TEC module. Through the use of a PI controller and PWM generator, the output current of the dc/dc converter will be continuously adjusted so that the actual TEC current tracks the desired current and minimum power loss in the power electronics device can be achieved.

The flowchart of Fig. 10 provides an overview of the minimum power loss controller operation.

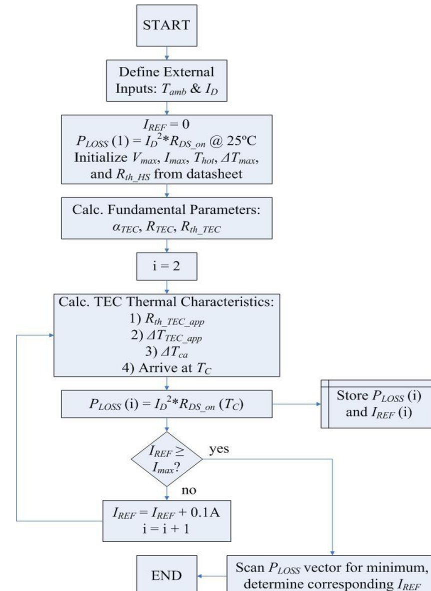


Fig. 10. Minimum power loss controller flowchart.

### D. dc/dc Converter

A 250 W dc/dc converter has been built to fit all the future work on TEC related topics. The dc/dc converter receives its control command from a DSP based controlled board. In the work that would be described by follow-up papers, the same controller board would be used to control the main power stage and the TEC module.

Fig. 11. 250 Watt dc/dc converter used to drive the TEC module.

### E. Simulation and Experiment Results

To validate the proposed minimum power loss control algorithm, an experiment is done to gather a group of power loss curves at different MOSFET drain currents. The results are then compared with those derived from simulation.

In the experiment, the drain current was set to a specific value and held constant while TEC current was swept in increments of 1.0 A starting from 0.0 A. For each value of TEC current, the system was allowed to stabilize for a minimum of 1.5 minutes to overcome the thermal time constant and ensure each reading had stabilized. As an example, one power loss curve at 15 A drain current is shown in Fig. 12. Fig. 12 shows the general agreement between simulated power loss and experimental power loss curve. There is a relatively large error in the low TEC current region which is due to the simplicity of the MOSFET power loss model. A comprehensive MOSFET model will be adopted in future works, which could get more accurate simulation results.

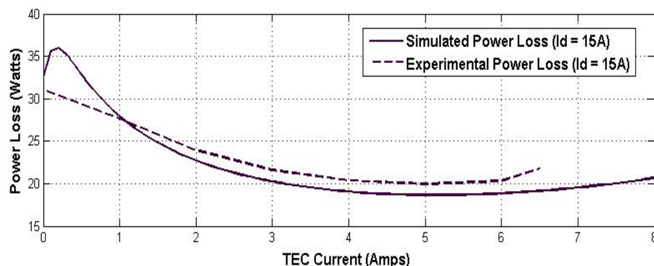


Fig. 12. Simulated power loss vs. experimental power loss at 15 A MOSFET drain current.

Table 1 shows the comparison of simulated and experimental minimum power loss and corresponding TEC current under different MOSFET drain current situations. It can be seen that, in this simulation, both the minimum power loss and TEC reference current agree with the experimental data very well. This result proves the validity of the proposed minimum power loss algorithm.

TABLE I
THE COMPARISON OF SIMULATED AND EXPERIMENTAL MINIMUM POWER LOSS

| $I_D$ (A) | EXPERIMENTAL $P_{LOSS_MIN}$(W) | SIMULATED $P_{LOSS_MIN}$(W) | EXPERIMENTAL $I_{TEC_MIN}$(A) | SIMULATED $I_{TEC_MIN}$(A) |
|---|---|---|---|---|
| 5 | 1.73 | 1.6288 | 5.0 | 4.8 |
| 10 | 7.77 | 7.4934 | 4.0 | 4.2 |
| 15 | 19.94 | 18.6514 | 5.0 | 5.1 |

## VI. CONCLUSION

This paper discusses the possibility and effectiveness of using TEC modules in the thermal management of power electronics devices. TEC based active cooling for power electronics has many benefits including compacted size, low weight, no acoustic noise and high reliability. A simple test setup in which MOSFETs are used as heat sources is built to compare the power losses of TEC based active power cooling and passive cooling. To maximize the benefits of TEC based cooling, a minimum power loss control strategy is proposed and validated by both simulation and experimental results. The minimum power loss control strategy proposed can be directly incorporated in an integrated system in which power electronics circuits and their cooling devices are jointly controlled to achieve a high power density. More detailed studies and further system developments would be reported in the follow-up papers.

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