# Recent Developments on High-Power Switched-Capacitor Converters

Ke Zou and Jin Wang*
Department of Electrical and Computer Engineering
The Ohio State University
Columbus,OH,USA
*wang@ece.osu.edu

*Abstract*—**This paper investigates the recent developments on switched-capacitor converters for high power applications. Based on an analysis on the shape of capacitor charging current for switched-capacitor converters, technologies used to improve the efficiency and reduce the Electromagnetic Interference (EMI), including the soft-switching and interleaving scheme, are discussed. Several existing topologies for high-power switched-capacitor converters are summarized and compared with respect to components stress and efficiency. A new voltage regulation method for high-power switched-capacitor converters is also introduced.**

***Keywords-*** *Switched-capacitor converters; soft-switching; interleaving opeartion*

## I. INTRODUCTION

The switched-capacitor (SC) circuit concept has been successfully applied in small-scale power conversions. The inductor-less feature of SC converters makes it especially suitable for chip-level power conversions. Various topologies and control methods have been proposed and successfully applied [1]-[4].

However, when it comes to high power applications, where high efficiency and low components stress are emphasized, many traditional SC circuit topologies and analysis methods are not applicable. On the topology side, many classic SC circuits either require large switching devices and capacitors, or may produce large peak charging current. To solve this problem, several topologies and control methods [5]-[10] have been developed in recent years to push the SC converter to higher power range. Each of the existing topologies possesses some advantages as well as some disadvantages. Sacrifices have to be made, either on the total switches and capacitor count, or on the efficiency of the converter.

Due to parameter differences, the shape of the capacitor charging current for a high voltage SC converter can be much different from a low-power SC converter. This feature enables many methods to increase the efficiency, reduce EMI noises and realize output voltage regulation through regulating the capacitor charging current. Two developments have been made to improve the efficiency of high-power SC converters. The first is a soft-switching method that does not require extra inductors, as proposed in [11]. By adopting this scheme, the switching loss is largely reduced and the capacitor charging current can be controlled, which results in a reduced EMI. The other development is the interleaving structure [11] to eliminate the large input current ripples and the associated conduction loss on the input capacitor.

The voltage regulation is crucial for a SC converter. However, traditional voltage regulation methods are based on a RC equivalent circuit of the capacitor charging loop, which decreases the converter efficiency and makes the converter unsuitable for high power applications. To solve this problem, a voltage regulation method based on a RLC equivalent circuit of the capacitor charging loop [15] is presented for high power SC converters, which can achieve higher efficiency than traditional methods.

This paper performs a survey of the recent developments on the topologies and control methods for high-power SC converters. Firstly, the shape of the capacitor charging current is analyzed under different loop impedance conditions. Then the soft-switching and interleaving methods that help to increase the efficiency of SC circuits are introduced. Different topologies are investigated and compared based on their requirements on components and their efficiency. A high-efficiency voltage regulation method is introduced at the end.

## II. THE CAPACITOR CHARGING CURRENT FOR SWITCHED-CAPACITOR CIRCUITS

One simple circuit to analyze the capacitor charging current is to lump all the parameters together to a simple series RLC circuit, as shown in Fig.1. In this circuit, $\Delta V$ represents the voltage difference between the voltage source and the capacitor being charged. The resistor R represents the total resistance in the charging loop, which includes the on-resistance of the semiconductor switches, the ESR of the capacitors, the stray resistance on the cables, and the internal resistance of the voltage source. The inductor $L_S$ represents the total stray inductance of the charging loop, which may include the cable stray inductance and the package inductance of the switches. The capacitor C represents the capacitance of the charging loop.

To solve this RLC circuit and find out the important factors, the charging current equations can be written as:

$$\frac{d^2(i(t))}{dt^2}+\frac{R}{L}\frac{di(t)}{dt}+\frac{1}{LC}i(t)=0. \quad (1)$$

The damping factor is defined as:

978-1-4577-1683-6/12/$26.00 ©2012 IEEE

$$\varsigma = \frac{\alpha}{\omega_0} = \frac{R}{2}\sqrt{\frac{C}{L}}. \tag{2}$$

The capacitor charging current can be expressed as:

$$i_c(t) = e^{-\alpha t} A \sin(\omega_d t), \tag{3}$$

In (3), the term $A\sin(\omega_d t)$ reflects the LC oscillation of the capacitor charging loop, in which $A$ and $\omega_d$ represent the amplitude and frequency of the oscillation, respectively. $\omega_d$ equals $1/\sqrt{LC(1-\varsigma^2)}$. The term $e^{-\alpha t}$ reflects the attenuation of the LC oscillation due to the loop resistance $R_S$. $\alpha$ is the attenuation factor and $\alpha = R_S / 2L_S$.

Fig.2 shows the shape of the capacitor charging current at different damping factors. With a large damping factor, the current waveform has a large initial value with the amplitude slowly decaying. With a small damping factor, however, the charging current has a waveform shape close to sinusoidal. For SC converters with smaller power ratings, the small size of components and cables results in a large loop resistance which dominate in the damping factor equation (2). While for converters with large current rating and thus large physical size, it is required for both capacitors to have low ESR and switches to have low on-resistance, so the efficiency can be guaranteed. Moreover, the loop inductance will also be larger due to the long connection cables. As a result, the loop resistance may not dominate in the charging current equation and the damping factor can be much smaller than 1, which results in a sinusoidal shape of charging current.

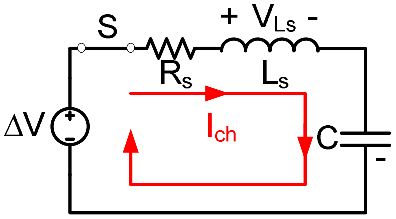

Fig.1. The RLC equivalent circuit for the current charging loop.

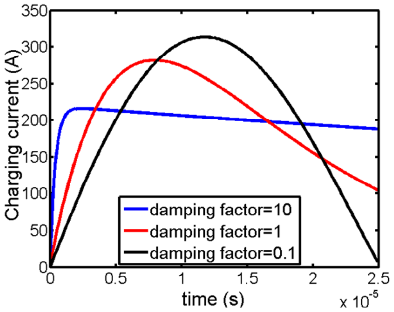

Fig.2. The capacitor charging current at different damping factors.

## III. Methods to improve efficiency in high-power switched-capacitor converters

### A. The soft-switching for large power switched-capacitor converters

From the charging current equation, it can be seen that if the damping factor is much lower than one, the charging current has a sinusoidal shape. If the switching frequency is adjusted to a proper value, the switching action will happen under zero-current condition. Therefore, the soft-switching (zero-current-switching) is achieved [10].

It is quite important for the charging loop to have sufficient capacitance and stray inductance to make the oscillation frequency small enough that can be achieved by existing semiconductor devices. The required switching frequency can be calculated:

$$L = \frac{1}{4\pi^2 f_0^2 C}, \tag{4}$$

where $f_0$ is the switching frequency.

It can be seen from (4) that the adoption of wide band-gap devices will significantly reduce the requirements on the capacitance and stray inductance.

### B. The interleaving scheme to increase efficiency and reduce output voltage ripple

A severe problem for traditional SC converters is the large input current ripple caused by the charging current. Even with the soft-switching technology, the sinusoidal shape of input current can still generate large conduction losses and requires an extremely large input capacitor to filter out these current ripples. The interleaving concept is to use several identical SC converter modules in parallel, with a constant phase shift between two modules. Small input current ripple and output voltage ripple can be achieved from this interleaving structure. One example is the multi-phase MMSCC presented in [11]. For a 4X MMSCC converter, the power loss of the input capacitor can be reduced to 4% of the loss without this interleaving scheme. Since the output voltage is also interleaved, the output capacitance can be largely reduced.

The main problems of this scheme are that excessive amount of components are required. This will increase the cost and the chance of component failure of the converter.

## III. A SURVEY ON HIGH POWER SWITCHED-CAPACITOR TOPOLOGIES

Based on how the electric charges are transferred from the source to the load, high-power SC converters can be divided into two categories: direct-charging based converters or indirect-charging based converters.

### A. Direct-charging based converters

Direct-charging means the voltage source directly charges the output capacitor. Since no intermediate stage exists in this type of converter, the number of capacitors can be minimized. Because the electric charges are directly sent from the source to the output capacitor, the conduction loss is minimized. However, for this type of SC converters, the power ratings of switches and capacitors are usually large, which makes them unsuitable for high power applications, especially for the high voltage transfer ratio conditions.

There are mainly two direct-charging schemes: the parallel-series converter and the converters based on time-sharing scheme.

### 1). Parallel-series converters

This is the simplest switched-capacitor converter scheme which has been widely used for decades. The switches in this converter are divided into two groups. When the first group of switches is turned on, all the capacitors are charged by the source in parallel, and when the second group of switches is on, all the capacitors are discharging to the load in series. As a result, the output voltage is boosted.

Despite its simplicity, this topology is not suitable for high-power applications. Because during its operation, the output voltage either equals the input voltage or N times the input voltage. This large voltage ripple yields an extremely large output capacitor requirement, which is not achievable for high-power applications.

### 2). Converters based on the time-sharing concept.

The time-sharing concept means the source takes turns to charge each output capacitor. If there are N capacitors needed to be charged, each capacitor is only charged for $1/N$ of the switching cycle. This scheme is ideal for realizing a voltage doubler, with the voltage stress of each switch equals the input voltage, and the duty ratio is maximized to 50%.

However, this time-sharing scheme is not efficient when voltage transfer ratio is higher than two. As the number of stages increases, both the voltage stress on the switches and the peak charging current will increase, which yield a higher converter cost and larger power losses.

A voltage tripler topology based on the time-sharing concept is shown in Fig.3. In this topology, all the switches need to either block two times the input voltage or block both positive and negative voltages. Moreover, since the capacitor charging duty ratio is only 1/3, the voltage tripler has a high peak current, which generates larger conduction losses.

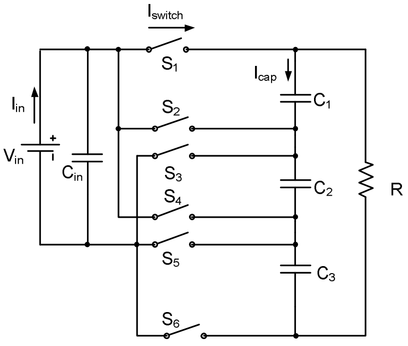

Fig.3. The direct-charging 3X converter topology.

## B. Indirect-charging based converters.

Indirect charging means that extra capacitors are added as the intermediate stages to help the energy transfer from the source to the load. Therefore, in this type of topologies, the electric charges need to flow in and out of the intermediate capacitors, which will increase the conduction loss. However, with the added capacitors, both the peak charging current and the required number of switches can be reduced.

### a). A magnetic-less bi-directional dc-dc converter

The first converter topology investigated is a bidirectional switched-capacitor dc–dc converter introduced in [5]. In this topology, a group of switching cells are used and each cell consists of two switches. Because all the switches have the same voltage rating as the input voltage, it is suitable for high voltage applications.

The main drawback of this topology is the large amount of components it requires. If one capacitor or one switch is defined to have a voltage stress of the input voltage, to realize a voltage conversion ratio of N, a total of N(N+1) switches and N(N+1)/2 capacitors are required. So this converter can only be used to achieve low conversion ratio converters.

### b). Flying capacitor multilevel dc-dc converter (FCMDC)

An improved structure is the flying capacitor multilevel dc-dc converter (FCMDC) shown in Fig. 3 [6]. In this topology, the number of switches is reduced to 2N. In [7], a control method is presented so three different levels of output voltage can be realized by a 3X converter using this topology.

However, it still suffers from several serious problems, including the high number of capacitors, unequal current stress of switches and reduced charging current duty cycle when the voltage transfer ratio is high.

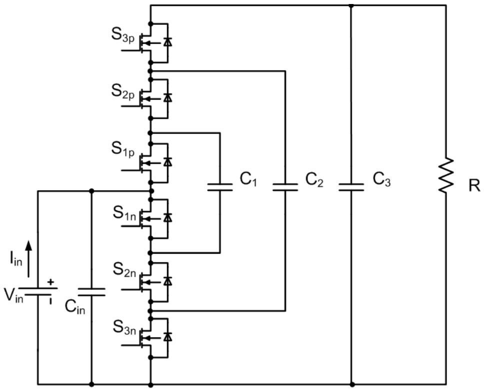

Fig.4. The FCMDC topology.

### c). Multilevel modular capacitive clamped dc-dc converter (MMCCC)

The MMCCC topology is presented in [7] and shown in Fig.4. It has many advantages compared to the previous topologies. The charging current duty ratio is always 0.5 regardless of the voltage conversion ratio, which results in a low conduction loss. The number of switches is only 3N-1 for a voltage conversion ratio of N.

However, the capacitor count is a large number, which equals to N(N+1)/2. Since the stress of capacitors in each stage is not identical, it is costly for this topology functions as a modular structure for high voltage applications.

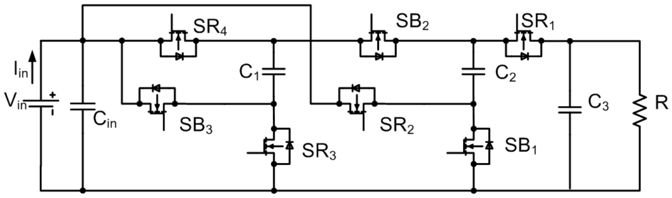

Fig.5. The MMCCC topology.

### *d). Switching-cell based dc-dc converter*

The switching-cell based dc-dc converter adopts a series of 'Marx cells'[9], which are derived from the traditional Marx generator in high voltage engineering. Both dc/dc and dc/ac operation can be achieved using this switching-cell concept. The soft-switching of the dc/ac inverter can be achieved by adopting a variable frequency control. The benefits of this topology includes: the modular structure, minimized capacitor count and the capability to achieve multiple output voltages.

The problems of this converter include its centralized structure, which causes unequal current stress of different stages. Moreover, the charging current duty ratio reduces as the voltage conversion ratio increases.

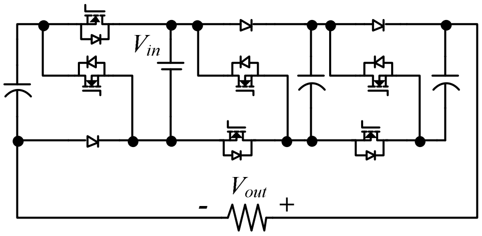

Fig.6. The 3X switching-cell based converter.

### *e). A converter topology with automatic interleaving function*

As discussed above, a good SC topology should have small capacitor and switch counts, a large charging current duty ratio, the zero-current-switching capability, and the interleaving capability to reduce the losses in the input capacitor. Fig.7 (a) shows a voltage tripler topology that can realize these functions without adding a large number of components.

There are three stages in this converter, with each stage consisting of two capacitors and four switches. A two-step charging scheme is used here. Take the top stage for example, in the first step, the voltage source charges $C_4$ through $S_1$ and $S_2$ for a half cycle. In the second step, $C_4$ charges the output capacitor $C_1$ through $S_3$ and $S_4$ for another half cycle. The duty ratio of the two steps is 0.5 so the charging current in the proposed circuit is always 180 degrees. All three stages have the same operation mode but with 120 degrees phase shift in between, so the interleaving operation can be realized.

Fig.7(b) shows the input current waveforms. The total input current ripple can be reduced more than 85% compared to the topology without interleaving operation. For this 3X converter, switches in the top and bottom stages have a voltage stress equals the input voltage, while switches in the middle stage have zero voltage stress. All the capacitors have a voltage stress equals to the input voltage. So the total components count is small.

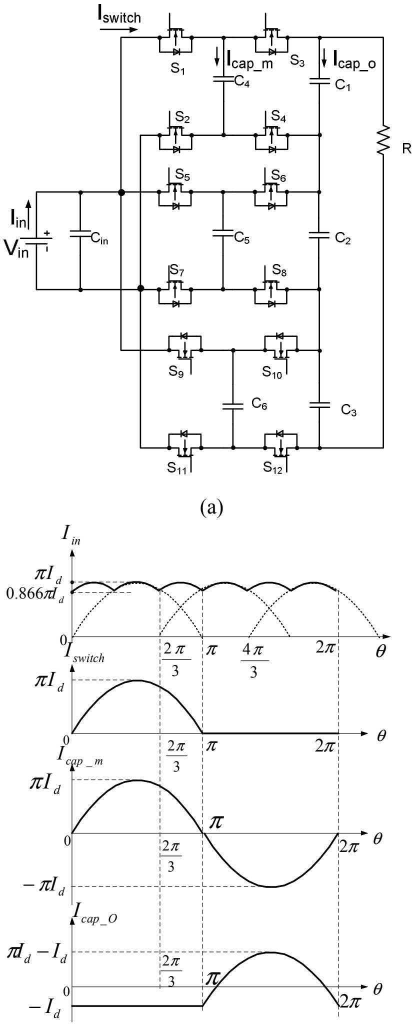

Fig.7. (a) A voltage tripler with automatic interleaving capability. (b) The input currents waveforms.

### *C. A comparison of existing topologies in dc-dc applications.*

To compare different topologies, three criteria are used here: the switch count, the capacitor count and the duty ratio of charging current. A smaller duty ratio of the charging current will results in a larger peak charging current and thus a higher conduction power loss. The capacitor count does not include the input capacitor. The comparison results are shown in Table I.

TABLE I. A COMPARISON OF SWITCHED-CAPACITOR TOPOLOGIES

| | No. of Capacitors | No. of Switches | Charging current duty ratio |
|---|---|---|---|
| Parallel-series | N | N(N+1)/2 | 1/2 |
| Time-sharing | N | 2N(N-1) | 1/N |
| FCMDC | N(N+1)/2 | 3N | 1/N |
| MMCCC | N(N+1)/2 | 3N-1 | 1/2 |
| Switching-cell based | N | N(N+1)/2 | 1/N |

## IV. A VOLTAGE REGULATION METHOD FOR HIGH POWER SWITCHED-CAPACITOR CONVERTERS

Traditional voltage regulation methods for SC converters adopt a RC equivalent circuit of the capacitor charging loop. As a result, the efficiency cannot exceed the normalized voltage transfer ratio [13]. For large power SC converters, the stray inductance $L_S$ of the capacitor charging loop may not be neglected. The capacitor charging loop can be represented by a series RLC circuit. If both $L_S$ and $R_S$ can be used to regulate the output voltage, the converter efficiency can be higher than traditional methods [14].

Fig.8 shows the shape of the capacitor current for an output capacitor in one switching cycle. The capacitor charging current has a sinusoidal shape with a decaying term $e^{-\alpha t}$. The initial angle of the sinusoidal current is $-\theta_0$, which is due to the fact that the capacitor continuously provides the load current. $\theta_1$ is the termination angle of the charging current.

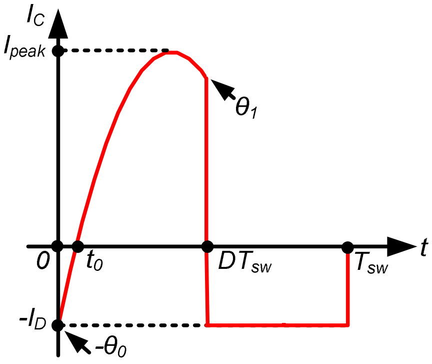

Fig.8. The shape of the capacitor current.

The voltage of the capacitor during the charging time can be expressed as:

$$\begin{aligned} V_C(t) &= V_{in} - R_S i_L(t) - L_S \frac{di_L(t)}{dt} = \\ & V_{in} - I_D R_S - \frac{R_S}{2} A e^{-\alpha t} \sin(\omega_d t - \theta_0) - L_S \omega_d A e^{-\alpha t} \cos(\omega_d t - \theta_0). \end{aligned} \tag{5}$$

$\theta_0$, $\theta_1$ and $A$ can all be calculated and expressed as a function of the duty ratio D. Therefore, by controlling the duty ratio D, the output voltage of the capacitor can be controlled.

Since the stray inductance is involved in the voltage regulation, the new method can achieve higher efficiency than traditional methods, which totally depends on the loop resistance to realize the voltage regulation.

## V. CONCLUTION

This paper reviews recent developments of high-power switched-capacitor converters. The feature of the capacitor charging current of high power SC converter is discussed. Two new control methods, including the soft-switching and interleaving method, are introduced. Several high-power switched-capacitor converter topologies are compared based on the components counts and the duty ratio of the charging current. The new method on the voltage regulation of SC converters is investigated.

## REFERENCES

[1] A. Ioinovici, “Switched-capacitor power electronics circuits,” *IEEE Circuits Syst. Mag.*, vol. 1, no. 3, pp. 37–42, 2001.

[2] H. Chung, “Design and analysis of a switched-capacitor-based step-up dc/dc converter with continuous input current”, *IEEE Trans. on Circuit & Systems*, vol. 46, no. 6, pp. 722~730, Jun 1999.

[3] C. K. Tse, S. C. Wong, and M. H. L. Chow, “On lossless switchedcapacitor power converters*,” IEEE Trans. Power Electron.*, vol. 10, no.3, pp. 286–291, May 1995.

[4] B.Arntzen and D.Maksimovic, “Switched-Capacitor DC/DC Converters with Resonant Gate Drive,” *IEEE Trans. on Power Electronics,* Vol.13, No.5, Sept.1998.

[5] F.Z.Peng, F. Zhang, and Z. Qian, “A Magnetic-Less DC-DC Converter for Dual-Voltage Automotive Systems,” *IEEE Trans. on Industry Applications,* vol. 39, no. 2, Mar. 2003, pp. 511-18.

[6] F. Z. Peng, F. Zhang, Z. Qian, “A novel compact dc-dc converter for 42V systems,” *IEEE Power Electronics Specialists Conference*, pp. 33-38, June 2003.

[7] Wei Qian, F.Z.Peng and L.M. Tolbert,; “Development of a 55 kW 3X DC-DC Converter for HEV systems”, *Vehicle Power and Propulsion Conference*, 2009, pp. 433-439.

[8] F.H. Khan, L.M. Tolbert, “A Multilevel Modular Capacitor Clamped DCDC Converter,” *IAS2006*, Oct. 2006.

[9] J.I.Rodriguez and S.B.Leeb, “A Multilevel Inverter Topology for Inductively Coupled Power Transfer,” *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1607-1617, Nov.2006.

[10] K.Zou,M.Scott and J.Wang, “Switched Capacitor Cell Based Dc-dc and Dc-ac Converters,” *APEC2011*,Mar.2011.

[11] D.Cao and F.Z. Peng, "A family of zero current switching switched-capacitor dc-dc converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC) 2010*, pp.1365-1372, 21-25 Feb. 2010.

[12] D. Cao and F. Z. Peng, “Multiphase Multilevel Modular DC-DC Converter for High Current High Gain TEG Application,” in *IEEE Energy Conversion Congress and Exposition 2010.* Atlanta, 2010.

[13] K. D. T. Ngo and R. Webster, “Steady-State Analysis and Design of a Switched-Capacitor DC-DC Converter”, *IEEE Transactions on Aerospace and Electronic Systems,* vol. 30, no. 1, pp.92–101, January 1994.

[14] K. Zou, Y. Huang and J. Wang, “A voltage regulation method for high power switched-capacitor circuits”, in *IEEE Applied Power Electronics Conference and Exposition 2012,* pp.1387 -1391, Orlando, 2012.