The Detection of DC Arc Fault: Experimental Study and Fault Recognition

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***Abstract*—DC arc fault introduces major safety concerns in a wide variety of power electronic applications. However, the randomness and instability of dc arc makes it difficult to be detected. In this paper, an experimental system to study the characteristics of series dc arc is designed and different tests were conducted in order to determine the influence of different factors to the arc such as gap length, current, etc. During the experiments, the load current was varied from 6 A to 30 A, and dc source voltage was changed from 75 V to 300 V. Also, dc arc test with fixed power supply voltage and load current but changing gap length were conducted to examine the influence of arc length. Based on the experimental results, a primary V-I characteristics study was carried out. Current variation analysis was performed to investigate the pulse patterns of the arc current for detection purposes. High frequency arc impedance under different test conditions was also investigated. Lastly, time frequency analysis was applied to the different arc current signals in order to examine the impacts of factors such as load current, dc bus input voltage to the arc current with respect to frequency domain. The results of this paper provide insights of the dc arc characteristics as well as methods for dc arc fault detection.**

I. INTRODUCTION

DC arc faults can occur in the electrical systems of electric vehicles, ships, aircrafts, photovoltaic plants, variable speed drives, utility energy storage units, and any other applications that involve high voltage dc buses [1-3]. If not detected and extinguished on time, the arc faults could spread to adjacent circuits and endanger the power sources, control systems, or even cause explosions in a confined space due to the growing arc pressure.

DC arc detection methods based on frequency analysis have been presented in [3-4]. In [3], back propagation neural network analysis is used along with a Fast Frequency Transform (FFT) method in order to detect dc arc in spacecraft systems. In [4], with wavelet packet based analysis, dc arc energy in different sub-bands is quantified into one variable by using the reconstruction coefficients in each band. These methods give insight into the frequency characteristics of a dc arc and also present the challenges in arc detection, such as noise recognition, calculation time reduction, differentiation from load changes, etc.

Besides frequency domain based detection methods, in [5] and [6], resonant circuits are used to detect dc arc by identifying high frequency oscillations produced by it. In [7], statistical methods are adopted to identify arc by studying the variance of the arc (voltage or current) signal. Lastly, in [8], for automotive applications, voltage and current sensors at two different locations in the electrical circuit are utilized to detect anomalies caused by dc arcs. Although many methods for dc arc detection have been studied, a simple, accurate, reliable and cost effective solution is still needed. To assist dc arc related standard development, more experimental supported theoretical studies of the characteristics of dc arc are also necessary.

Based on the location with respect to the load, the arc faults can be classified into two types: series and parallel. Between these two types of faults, the series arc faults are more common. Thus, it will be the focus of this paper. Series arc faults are often caused by loose connectors, terminals and so on [9]. In this paper, a series dc arc test setup is designed and built to study the dc arc phenomenon. Both current variation analysis and wavelet based time-frequency analysis are applied to investigate the characteristic of the dc arc. Based on the analysis, signatures for dc arc fault recognition can be established.

II. ARC CHARACTERISTICS

A. Setup and Test Procedure

Table I summarizes the experimental conditions for dc arc tests. The copper electrodes used for arc generation are rod-type with a cross section of 0.252 inch in diameter. Before each test, the surface of the electrodes was polished in order to remove the burns from last arcing. A step motor was applied to separate the two electrodes at a constant speed. In this

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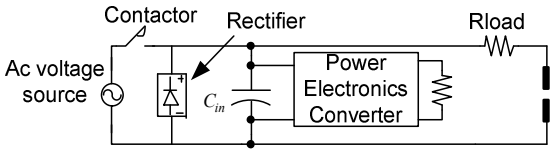
study, the anode rod is held stationary while the cathode rod moves apart. The power supply is composed by a high power variac and a rectifier unit. The load is a variable resistive load bank in parallel with a boost converter which could be controlled to inject controlled noise at different frequencies. Fig. 1 (a) shows the arc generating unit and a free burning arc and Fig. 1 (b) shows the diagram of the entire experimental setup.

TABLE I. EXPERIMENTAL CONDITION

Electrodes material	Copper
Load type	Adjustable resistance
DC source voltage	75 V, 120 V, 175 V, 240 V, 300V
Load current	3 A, 6 A, 15 A, 25 A
Gap length	0.06 in, 0.07 in, 0.08 in, 0.095 in, 0.12 in, 0.14 in

(a) Arc generating unit



(b) Diagram of the experimental system

Figure 1. Schematic diagram of the experimental system.

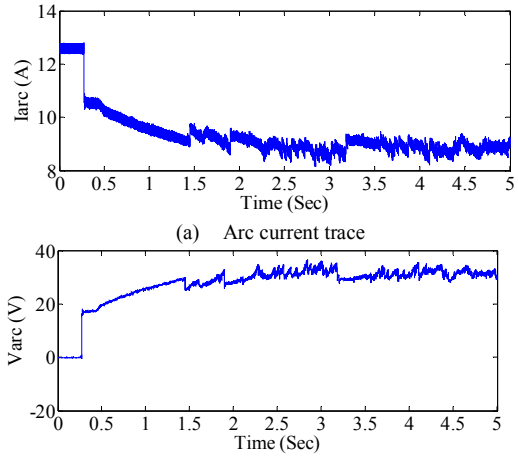
In order to examine the influence of dc source voltage and load current on dc arc, both changing voltage and current tests were carried out. The experimental procedure is as follows. At first, the dc source voltage is set at 75 V and the load current is controlled to be 3 A, 6 A, 15 A, and 25 A by adjusting the load resistance. Then, the dc source voltage is increased to 120 V and the above 4 load current levels are adjusted again successively. The same procedure is repeated for 175 V, 240 V and 300V dc source voltage.

To investigate the relationship between arc resistance and gap length, dc arc tests with fixed voltage and current but changing gap length were also conducted. During this set of tests, the dc source voltage is maintained at 80 V while the load resistance is maintained at 12 Ohm to achieve the same load current. DC arcs current and voltage were measured under the following 6 different gap lengths: 0.06 in, 0.07 in, 0.08 in, 0.095 in, 0.12 in and 0.14 in.

Lastly, in order to study the V-I characteristics of the dc arc, a set of tests were conducted in which the dc voltage was maintained at 80 V. The gap length was set at 0.08 in while the load resistance was adjusted to achieve different load current levels. The test results were used to analyze the V-I characteristics.

All of the arc signals, including arc current and arc voltage, were recorded using the YOKOGAWA DL850V digital scopecorder. This scopecorder has an analog to digital conversion resolution of 16 bits and the sampling rate used for the tests is 200 kHz. The recording length was 5 seconds although the arc faults lasted longer. Both the onset of the arc and the stable arcing were recorded.

Fig. 2 shows an example of measured arc voltage trace and arc current trace. In this particular example, the dc source voltage is 80 V with a load current of 12.5 A. The rise of the arc voltage and the fall of the load current (arc current) indicate the initiation of the arcing process.



(a) Arc current trace

(b) Arc voltage trace

Figure 2. Arc current trace and arc voltage trace.

B. *Arc Resistance*

Fig. 3 shows the average arc resistance versus dc source voltage, under different circuit current levels.

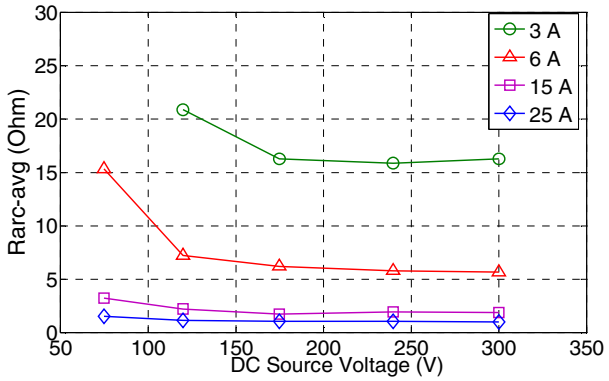


Figure 3. Average arc resistance

It can be seen that the dc source voltage has a slight influence to the arc resistance. The load current has a more

significant influence on the arc resistance especially when the current is low. The data point for 75 V dc source voltage and 3 A load current is not included in this figure since the arcing under this condition is not self-sustainable. Thus it is not comparable to the other data points which are from steady arcing.

C. *Arc Voltage*

A plot of the arc voltage versus dc source voltage is given in Fig. 4. In this figure, similar to the arc resistance, the arc voltage shows a stable flat trend with the increase of external dc source voltage.

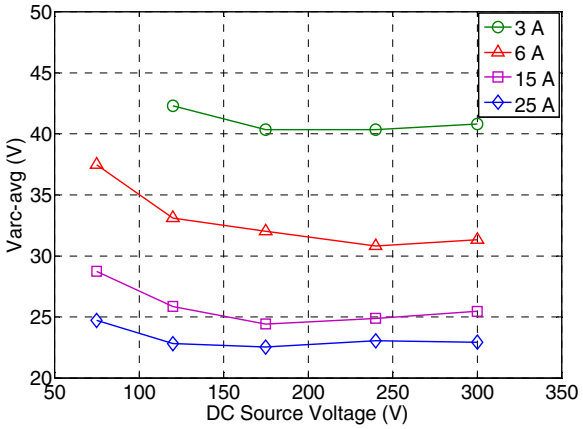


Figure 4. Average arc voltage.

Standard deviation was applied to investigate the influence of dc source voltage and load current to the arc voltage. For each load current level, the standard deviation of the arc voltage under the 5 different dc source voltage is calculated for all the 5 gap lengths, as shown by the error bar plotting in Fig. 5. Moreover, the error bar of the standard deviation for the 4 current levels is computed, shown in Fig. 6

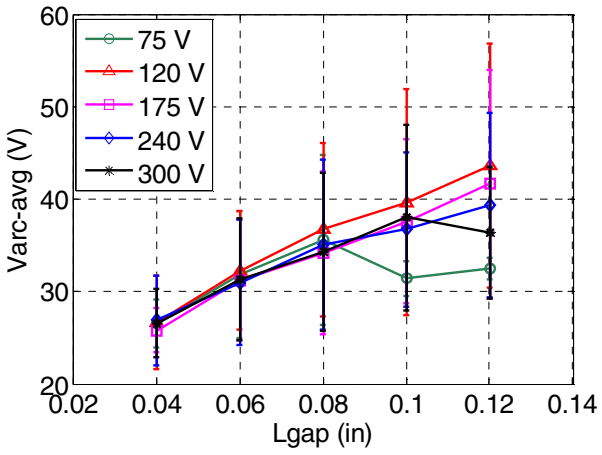


Figure 5. Arc voltage averaged over 5 voltage levels

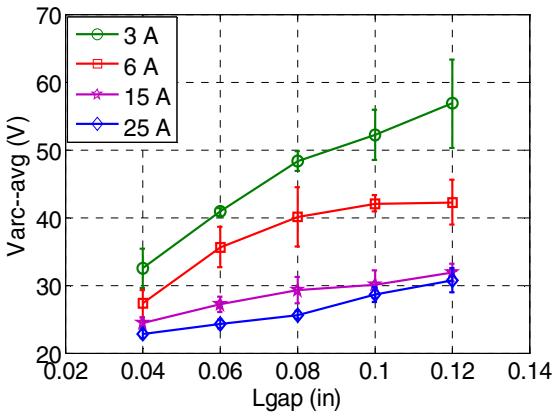


Figure 6. Arc voltage averaged over 4 current levels.

The curves in Fig.5 show an overall trend of arc voltage getting higher with larger gap length under all load current levels. The length of the error bar shows how the arc voltage at different dc source voltage is different from each other. There is clear gap between each curve which indicates a strong dependence of arc voltage to arc current. The shorter error bars at higher currents mean the arc voltage does not change much for different dc source voltage when the load current is high. This can also be verified by the overlapping of all the curves in Fig. 6. It is important to note that the data points for 75 V, at 0.1 in and 0.12 in are abnormal from the overall trend, which is again because the arc is not self-sustained at that voltage level.

D. *V-I Model of Arc*

As a complex physical phenomenon, an equivalent arc model has been under investigation since 1930s in order to better understand the arc behavior. Generally, there are two modeling approaches. One is numerical method using finite element analysis [10][11]. This approach applies a set of equations describing the physical process of dc arc such as the thermal dynamic and dielectric property using microscopic parameters. Finite element calculation is conducted based on the set of equations. This kind of model is adopted more for understanding the physical characteristics of the arc, in order to generate or control an arc for special utilization purposes, such as dc arc torch, plasma for material processing. The other approach is external characteristic model describing arc with a macroscopic equation to represent the electrical behavior of arc [12][13]. This method is more for understanding arc behavior as part of a system, such as the arc detection discussed in this paper. This approach requires large number of experiments to extract the proper V-I equation in a statistical way. It was found out that the V-I equations change significantly under different arcing conditions. Factors such as current level, temperature, gap length will influence the V-I equation. Thus, before an overall equation that could include all cases of arcing condition is obtained, more accumulation of experimental results and according model is desired. This

subsection is focused on the V-I characteristic modeling arc electrical behavior under the specific arcing condition involved in this study.

The arc voltage at different gap length and load current level is shown in Table II. The arc voltage value in Table II is obtained by averaging the arc voltage under the 5 different dc source voltages. From the previous analysis of the dc source voltage impact, the conclusion that the influence of dc source voltage is negligible in time domain analysis is assumed here.

TABLE II. ARC VOLTAGE AT DIFFERENT GAP LENGTH AND LOAD CURRENT

	3 A	6 A	15 A	25 A
0.04 in	32.5600	27.3146	24.4735	22.8526
0.06 in	40.8396	35.6210	27.1918	24.2715
0.08 in	48.2458	40.1064	29.2487	25.6249
0.10 in	52.1582	42.0752	30.1503	28.5911
0.12 in	56.7833	42.1882	31.9032	30.6755

A V-I characteristic model of the arc is proposed to quantify the relationships and trends mentioned above based on the following form:

$$V_{arc} = \frac{a}{I_{arc}^{\ b}} \qquad (1)$$

To incorporate the influence of gap length in the model, curve fitting is applied to the arc voltage and load current under each gap length. The curve fitting results are shown in Table III.

TABLE III. VALUES OF A AND B

	0.04 in	0.06 in	0.08 in	0.10 in	0.12 in
a	38.28	54.30	67.81	72.66	78.38
b	0.1660	0.2496	0.3036	0.3055	0.3165

From Table III, we can see that for gap length L=0.08 in, 0.10 in, 0.12 in, the V-I model shows more consistency, and is selected for gap length incorporation. By fitting the values of a and b to the gap length L, the following models could be achieved.

$$V_{arc} \frac{264.3 * L + 46.52}{I_{arc}^{\ 0.3055}} \qquad (2)$$

In order to verify the accuracy of the above model, the arc voltage using Eq. 2 is calculated and is plotted in Fig. 7 along with the measured value. From Fig. 7, we can see that most of the calculated numbers correspond well with the measured numbers. The largest error comes from arc at 0.04 in, 3 A and 6 A, this is because the characteristic model selected is from larger gap length. Nevertheless, the error is within 10% from the measured value.

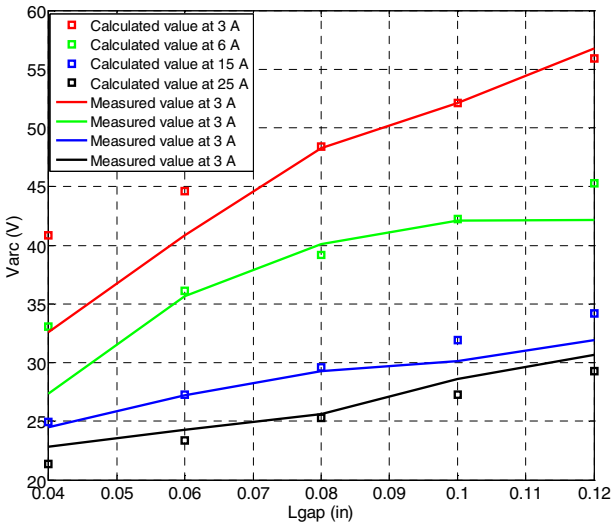


Figure 7. Arc voltage from V-I characteristic model.

III. TIME DOMAIN BASED CURRENT VARIATION PATTERN ANALYSIS

The physical processes of dc arc are both chaotic and dynamic. The arc current and arc impedance waveforms are consistently changing, influenced by the evaporation process and combustion of the electrode material, and also influenced by the magnetic field generated by the arc current itself when the arc current is large enough [9]. The chaotic characteristics of the dc arc current are reflected by the pulsed pattern of the current waveform: the current amplitude changes dramatically in a short period. Researchers have been looking into the chaotic characteristics of dc arc [7]. However, these methods involve complex computational procedures.

Thus, in this section, a simple yet effective method, which could be realized with low-cost detectors, is proposed to utilize the chaotic characteristic of dc arc for fault recognition purposes. First, a proper time window T_s is selected, then the maximum and minimum current amplitude I_{max} and I_{min} within each T_s is identified. The difference between I_{max} and I_{min}, I_{dif}, is calculated. The time window should be carefully selected to be long enough to represent current randomness appropriately but it also should not be so long as to reduce the sensitivity. Based on the sampling rate (200 kHz) and several trial calculations, T_s=10 ms is selected.

Fig. 8 shows the current variation patterns based on the arc traces shown in Fig. 2. The current variation shows three different patterns for different arcing stages. Through the whole arc burning period, an offset of around 0.4 A of I_{dif} is observed. This offset is caused by the ripple of the dc voltage generated by the rectifier and is not related with the arc characteristics. When the arc starts, a large I_{dif} is produced by the current drop, which could be a signature of dc arc but would require proper discrimination from the normal current

change caused by load transients and switching operations [1]. During the arc developing stage, when the electrode was moving, I_{dif} is low and smooth. When the electrodes stopped moving, the current variation pattern shows that the self-sustained arc has high I_{dif} values. The amplitude of the current variation can reach 1A. A possible explanation of this phenomenon could be the motion of cathode spots [9]. The cathode spots show higher mobility when the arc is continuously burning. These repeating yet unique large I_{dif} pulses could be used to indicate the occurrence of an arc fault. Therefore, I_{dif} could be chosen as one signature of dc arc fault.

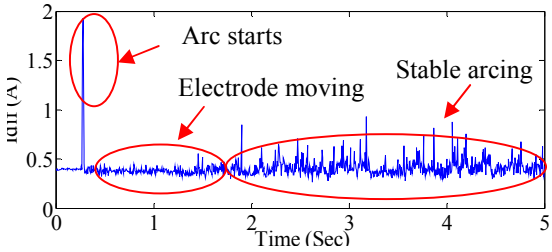


Figure 8. Current difference at different arcing stage

The average current variation under different dc source voltage and load current level is presented in Fig. 9. In order to eliminate the unwanted low frequency and high frequency noise from measurements, a hardware band pass filter was applied here. The bandwidth of this filter is 1.5 kHz – 45 kHz. The current variation analysis was applied to the filtered arc current signal. Results in Fig. 9 show that both the dc source voltage level and the load current level have influences to the arc current variation. For higher load current level, the current variation is larger. Moreover, the current variation tends to decrease with higher dc source voltage which indicates that although the dc source voltage has little impact on the arc voltage and arc resistance, higher dc source voltage has the ability to stabilize the arc current and make the current variation lower.

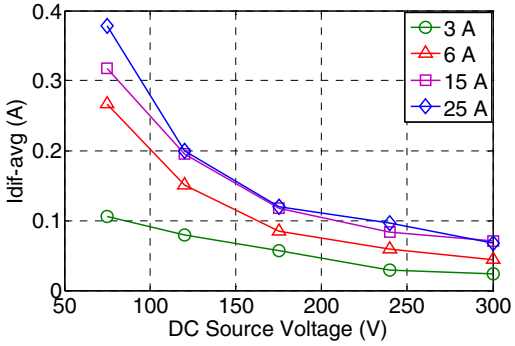


Figure 9. Average current variation at different dc source voltage and load current level.

IV. Arc Impedance Analysis in Frequency Domain

A. Impedance Analysis

To investigate the characteristics of arc impedance in the frequency domain, Fast Fourier Transform (FFT) is utilized. FFT was applied to both arc voltage signal and arc current signal, and then divide the two frequency spectrum to obtain the spectrum of arc impedance. Window averaging was applied to smooth the spectrum. The spectrum of arc impedance under 240 V tests is shown in Fig. 10 as an example. The spectrums for other dc source voltage tests are quite similar.

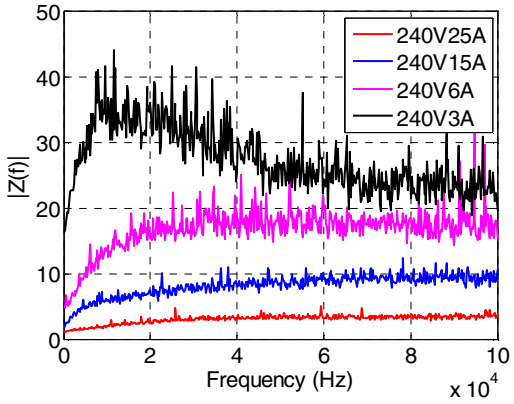


Figure 10. Arc impedance vs. frequency.

Fig. 10 shows that the arc impedance is very high at high frequency. This characteristic has important meanings to arc detection because it promises the possibility of detecting dc arc fault by monitoring the ripple change in power converters such as boost converter. The influence of arc fault to ripple current would have two terms. One influence comes from average arc voltage. Taking boost converter as an example, the average voltage drop on the arc will decrease the input voltage to the converter, thus cause reduction in current ripple. The other influence comes from the arc impedance at switching frequency. These two factors combined would change the current ripple significantly, which can be distinguished from the current change caused by changing load, and thus could be a promising arc detection signature.

B. Experiment verification

An experiment was conducted to verify the ripple changing during arc. The test setup is modified by adding a boost converter before the load resistance. The duty ratio of the boost converter is set at 0.5. The dc source voltage is 175 V, and load current is around 20 A. The inductor current is shown in Fig. 11, which shows 5 different arcing stages. Stage 1 is pre-arcing stage. Then the arc gap opens at 1.36 s which forms stage 2. However the arc does not happen immediately. This is because of the output capacitor of rectifier and input capacitor of boost converter. These two capacitor clamps the voltage across the gap in a low value which is not sufficient to initiate arcing. Stage 3 starts at around 1. 4 s when the voltage of the boost converter input capacitor decays to certain value which initiates the arcing. However, the arcing at this time is not stable because the electrode is still moving and the arc extinguishes at 1.47 s which starts stage 4 and reignite at 1.58 s and burns stably after that which forms stage 5. An obvious difference of the

ripple current could be observed between the inductor current at stage 1 before opening the gap and that at stage 5 when the arcing is stabilized.

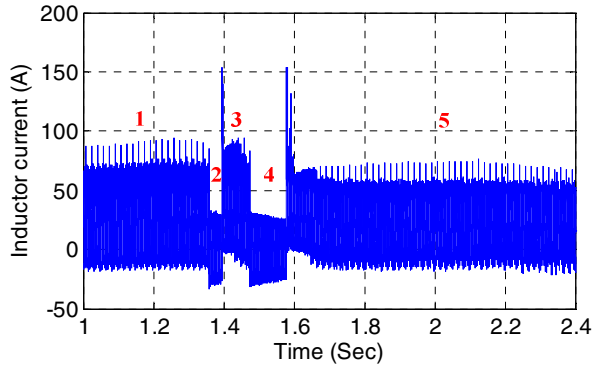


Figure 11. Inductor current of a boost converter before and during arcing.

V. TIME-FREQUENCY ANALYSIS

The main purpose of time-frequency analysis of the dc arc current is to understand the frequency characteristics of the current before and during arcing. Discrete Wavelet Transform (DWT) is the main method chosen in order to explore these features. Wavelets are commonly used in a variety of applications ranging from image compression, signal de-noising, to feature extraction and fault detection [14]. DWT is a form of multi-resolution analysis which states that any signal in the space of square integrable functions, can be written as a linear combination of a countable orthonormal basis, known as the "mother wavelet";

$$x(t) = \sum_{k=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} d_{k,n} . \psi_{k,n}(t) \qquad (3)$$

$$x(t) \in L_2,\ \psi \in L_2$$

Where the index *'k'* represents the level of decomposition of the signal and *'d'* can be interpreted as a representation of the signal in the *'k^{th}'* subspace. The coefficients, *'d,'* are obtained through low pass and high pass filters, *h[n]* and *b[n]*, which are dependent on the type of wavelet used. By passing a signal through these filters, a type of filter-bank analysis is formed, which gives the representation of the signal in different frequency ranges halved each time the signal is passed through these filters (caused by dyadic stretches of the mother wavelet) [15].

A. Types of Signals

Two types of series dc arc current will serve as models for the time-frequency analysis presented: a waveform containing a noise generated by a 20 kHz nearby power electronics converter, and another is a current waveform without intentionally added noise. In order to analyze the frequency characteristics of the current, only the ac components of the arc current were recorded. The waveforms are shown in Fig.12 (20 kHz noise) and Fig. 13 along with a spectrogram for the highlighted section of the signal.

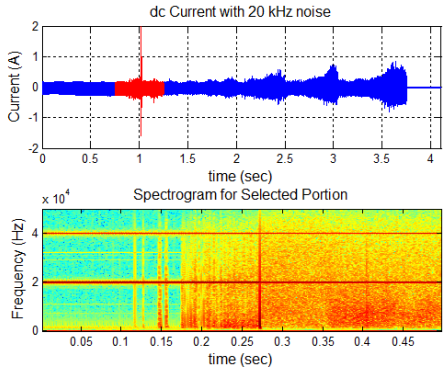


Figure 12. Arc current with 20 kHz added noise and its spectrogram

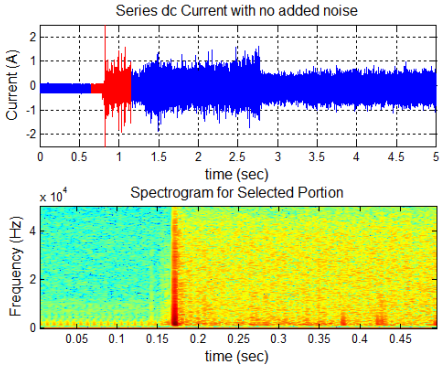


Figure 13. Arc current with no intentionally added noise and its spectrogram.

From the spectrogram representation of these signals in the designated section, it is possible to see how during the arc, an amplitude increase in all frequencies occurred due to the randomness and variation of arc current. This is the main reason why Wavelet Packet (WP) decomposition can be used in order to detect these increase in energy in the dc arc current.

B. Wavelet Packet Decomposition

The method presented for analyzing the arc current is a WP decomposition and examination of the Root Mean Square level in different sub-bands. The procedure follows dividing the signal into time windows *T* of 10 ms for a sampling frequency of 200 kHz and 20 ms for a sampling frequency of 100 kHz. WP decomposition (level 3) is performed using Daubechies 8 and Coiflet wavelets and the RMS value in each terminal node (*j=0..7*) for window (*T*) is calculated as follows:

$$e_j(T) = \left(\frac{1}{N} \sum_{n=1}^{N} {c_{j,n}}^2 \right)^{\frac{1}{2}} \qquad (4)$$

where *N* is the total number of coefficients in the j^{th} node. Lastly, the results in one of the frequency bands (node (3,1) to (3,7) ignoring dc part (3,0)) is then selected depending on the type of signal. Figures 12 and 13 show the cases for each type of current signal (with and without power electronics noise). This procedure is different from the procedure in [4], such as in the method for calculation of the features at each terminal node of the WP (RMS value is used in this paper).

From Figures 14 and 15, it is possible to see features that clearly distinguish dc arc in the selected frequency band, which can be chosen depending on the type of signal studied. Before the arc occurs (0~1s) the RMS of each signal is very low and consistent, however, once arc happens, the RMS increases in both signals and follows a pattern similar to the contour or outline of the signal. This increase in RMS value presents characteristics which can make the detection of arc easier.

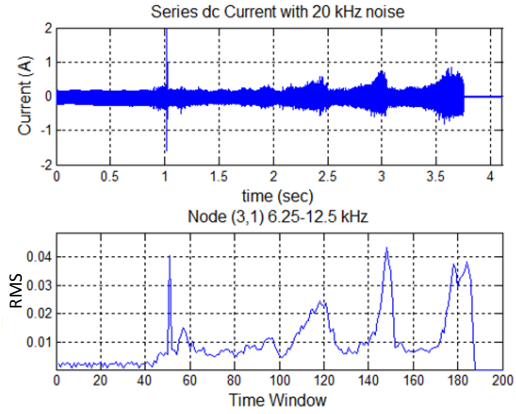


Figure 14. Arc current with 20 kHz noise and sub-band analysis.

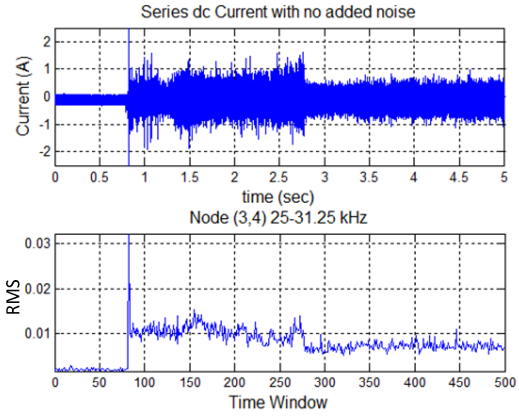


Figure 15. Arc current with no added noise and sub-band analysis.

C. *Influence of External Inputs*

From the circuit shown in Figure 1b, factors such as dc input voltage and load current have an impact on the characteristics of the dc arc. This influence can be studied by using the WP method described in the previous section. Fig. 16 shows a period of stable burning of the arc under voltage variations, with a fixed load current of 25 A. From this figure, it is clearly seen that the dc bus input voltage has an impact on the RMS level of the arc in the frequency bin of 37.5 to 50 kHz. The lower the input voltage the higher the RMS value of the arc, while the higher input voltage (e.g. 300 V) decreases the RMS level of the burning arc which in turn increases the level of difficulty for differentiation between arc and normal current.

Fig. 17 illustrates a stable arc current varying from 3 A to 25 A. However, there still appears to be a pattern in the effect of the current to the RMS level variation in this frequency range; the lower the arc current, the lower the RMS value of the signal while the higher arc current, the higher the RMS level of the signal. Nevertheless, the impact of load current is not as drastic as the input voltage impact. Comparing Figure 16 with 17, interesting enough, on contrary to the time domain analysis, for RMS level at high frequency region, the impact from the load current is not as notable as the impact from the dc bus input voltage.

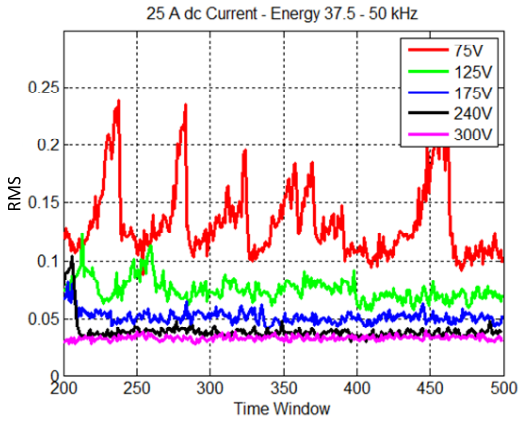


Figure 16. Impact from input dc voltage for fixed load current.

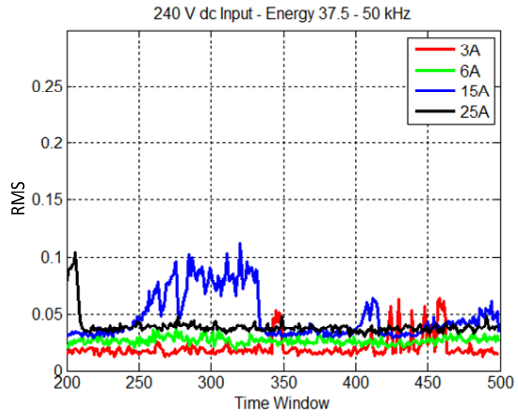


Figure 17. Impact from load current for fixed input voltage.

Similar patterns of RMS level variation occur under different voltage and current combinations. This study allows for the selection of thresholds for detection of dc arc based on a different range of input voltage and load current.

VI. Conclusion and Future Work

DC arc at different currents, voltages, and gap lengths were measured and analyzed in this paper. The test results show that the arc resistance stays stable with the increase of dc source voltage while it shows a strong dependence to the load current. The arc voltage also shows a loose relation with the dc source voltage especially when the load current is lower.

With the test results of changing gap length, it is noticed that the arc resistance increases with the increase of gap length.

The variation of arc current signals was analyzed as a simple and cost-effective method to indicate the occurrence of dc arc faults. A simple calculation procedure of the arc current variation was carried out to represent the chaotic and dynamic nature of the dc arc physical process. The current variation indicates different stages of the arcing and could be utilized for dc arc fault recognition. The average current variation value for different dc source voltage level and load current level was also analyzed. The results show that the current variation decreases with the increase of dc source voltage especially when the load current is higher. This indicates that although the dc source voltage has little impact on the arc parameters such as arc voltage, arc impedance, higher dc source voltage could suppress the chaotic nature of dc arc in certain degree and make the arcing more stable.

Arc impedance at high frequency domain was investigated. Results show that besides the high dc impedance, arc also exhibits high impedance at higher frequency. This high frequency impedance could cause impact on the current ripple of power converters, which would become an efficient detection signature to distinguish the arc from normal operations, such as load changing.

Lastly, characteristics of the arc current were discussed using spectrogram and a wavelet packet filter-bank. By analyzing the signal before and during arcing, it is possible to see how the random nature of the arc affects the frequency components of this signal. Furthermore, the RMS level analysis in different frequency bins show an inverse relation between the dc bus input voltage and the RMS level of the signal and a direct relation between the load current and RMS level. These results confirm the impact of the dc bus voltage previously stated; in which decreases the chaotic nature of the arc. Furthermore, this analysis can be applied in order to create features for dc arc detection.

The time domain analysis is based on the chaotic nature of the physical processes of arcing and provides an effective signature to indicate the occurrence of dc arc and different arcing stages with simple calculations. The latter provides additional signatures for dc arc from a time-frequency point of view. From the WP analysis, it is seen that the dc bus input voltage can have an impact in the RMS value variation of the arc current for a certain frequency.

In summary, this paper provides both experimental study and characteristics study of dc arc. The former forms a solid foundation for people's knowledge of the complex dc arc phenomenon while the latter provides guidance and methods for dc arc fault recognition.

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