A New Converter Topology for Advanced Static VAR Compensation in High Power Applications

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Abstract- Two generic configurations of forced commutated PWM converters, i.e. voltage source inverters and current source inverters, have been proposed as advanced reactive power compensators. A new configuration to combine the features of the two generic ones is proposed, designed and analyzed in this paper. It is composed of a PWM current source inverter handling high power with very low switching frequency, and a PWM voltage source harmonic filter handling low power with a much higher switching frequency. The result is that switching losses and harmonic distortions are both minimized simultaneously.

I. Introduction

Reactive power control is traditionally realized by connecting or disconnecting capacitor or inductor banks to the bus through mechanical switches, which are slow and imprecise. Solid-state VAR compensators using naturally commutated semiconductor devices such as thyristors and GTOs have also been developed [1,2], in which semiconductor devices functioned simply as a replacement of mechanical switches. A totally different approach is to use force-commutated converters to achieve advanced reactive power control based on energy storage principle. Pulse width modulation (PWM) is used to suppress low frequency harmonics and to reduce the size of passive storage elements. Other advantages of advanced static VAR compensator (SVC) include flexible, fast and precise reactive power control, better waveforms and multiple functionality.

Two classes of PWM inverter SVC have been proposed: SVC using PWM voltage source inverters (VSI) [3] and SVC using PWM current source inverters (CSI) [4]. Their behavior when providing leading reactive power and when providing lagging reactive power is not uniformly satisfactory. For example, harmonic performance of both the VSI and the CSI type SVCs depends on the direction and amount of reactive power flow [5]. The selection between the two general types of SVC depends on applications. For high power utility application, when efforts are made to meet the requirements of low switching losses and low harmonic distortion, the CSI seems more suitable than VSI since with high power GTO devices switched at a low frequency, the harmonics can be controlled to a reasonable level. Further improvement on harmonic distortion by raising the switching frequency is unrealistic because high power, fast switching devices are not available at present. Switched at a low frequency, the VSI type SVC generates unacceptable harmonic currents. Although the harmonic currents can be alleviated by raising switching frequency, the power rating of VSI is restricted by the available power transistors. It is evident that CSI or VSI alone can not provide satisfactory solutions to the high power, high efficiency and low harmonic static VAR control to power systems and utilities.

A new converter topology of SVC system is proposed in this paper, which is composed of a simple CSI handling high power with a very low switching frequency and a PWM VSI harmonic filter handling lower power with a much higher switching frequency. Both inverters use harmonic elimination PWM switching patterns, and the reactive power is controlled through a closed-loop phase-shift control.

In addition to functioning as a voltage support for the CSI, the VSI also filters out the unwanted lower order current harmonics produced by the CSI. Different from the PWM active filter techniques that regulate the converter current to optimally inject or compensate for the harmonic currents [7,8], a technique that provides short-circuit path for the harmonic currents is designed.

This advanced reactive power compensator has the potential of high performance and high reliability, and is particularly suitable for high power applications both in power systems and utilities.

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II. Configuration of the New System

The configuration of the new advanced SVC consists of a PWM voltage source inverter and a current source inverter with a open-circuit protection circuit, as shown in Fig. 1. The outstanding reason for the new configuration is the following appealing scenario: the CSI is controlled with a very low switching frequency and handles the bulk reactive power flow, while the VSI functions as an active filter with a much higher switching frequency.

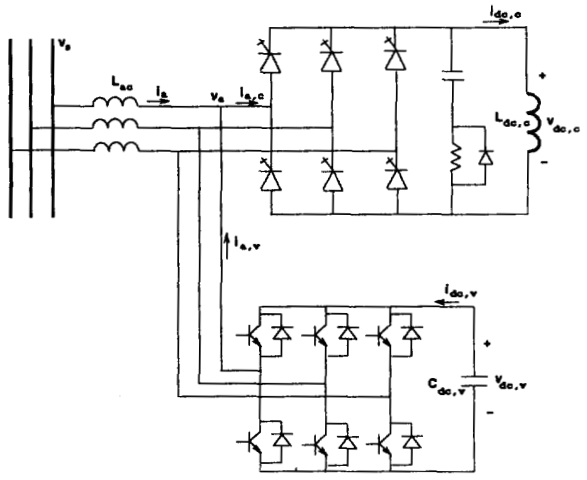

Fig.1 An Advanced VAR Compensator

Note that since the VSI is controlled as an active filter, its frequency spectrum profile can be shaped to the form that the VSI sinks completely the harmonic currents of concern, while drawing zero fundamental current.

The amount and direction of reactive power flow are controlled by the closed-loop phase-shift controller of both the VSI and the CSI, as explained in later sections. No other external control of both the dc buses is necessary. The switching patterns of both the VSI and the CSI are fixed and stored in EPROM, with no need for real-time computations.

III. Operation and Control of CSI

A. *Principle of Operation*

The CSI is responsible for providing, on its ac side, the required amount of reactive current, which is modulated to lead or lag the ac side voltage by approximately 90°. The current magnitude controls the amount of reactive power flow through the converter.

The magnitude of the phase current is controlled by changes in dc current, which in turn is adjusted by the level of the dc voltage. When the phase angle is not 90°, real power will flow through the converter, resulting in a non-zero dc reactor voltage. Thus the dc voltage is controllable through the gating phase angle control around negative or positive 90°, for leading or lagging VAR operation mode respectively. For leading VAR operation, when the phase angle is decreased from negative 90°, the dc voltage will be negative, resulting in a decrease of the dc current (hence the reactive power). For lagging VAR operation, when the phase angle is decreased from positive 90°, the dc voltage will be negative, decreasing the reactive power.

Even at steady state, the phase angle between the current and the phase voltage is not exactly ±90°, since a small yet adequate amount of real power is needed to compensate for the switching losses and other losses of the converter.

B. *Switching Scheme Generation*

As pointed out previously, only harmonic currents flow through the PWM VSI. Furthermore, by applying low frequency PWM in the CSI, certain lower order current harmonics through the VSI can be eliminated or minimized.

Unlike the PWM VSI, there are a limited number of switching schemes for the PWM CSI, due to its requirements of current symmetry and overall current continuity. In other words, these inherent constraints require that at any time, three phase currents sum up to 0 and one of them is 0. It's also possible that three phase currents can all be 0 at some instants.

The two schemes best satisfying these requirements are trapezoidal-triangle PWM and programmed PWM.

Programmed PWM stores pre-calculated patterns which attenuate selected low-order harmonics, while restricted by the current sum constraints. Let M be the number of chops within the 90°region and $\alpha_m (m = 1, ..., M)$ denotes angle positions of the chops. Fig. 3(a,b) show constraint satisfying switching patterns for an odd M and an even M, respectively. Note that these patterns for CSI are different from those of a harmonic elimination PWM for a voltage source inverter.

Using quarter-wave symmetry, from Fourier analysis, with Fourier coefficients denoted as a_h and b_h where h is the order of the harmonic of interest, it can be shown that for an odd M,

$$a_h = \frac{4}{h\pi}[\frac{3}{2} + \sum_{m=1}^{M}(-1)^m cos(h\alpha_m)$$

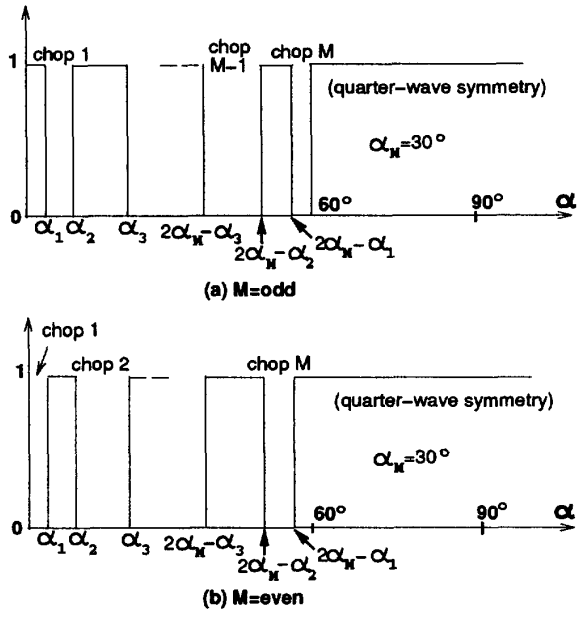

Fig.2 PWM CSI Switching Pattern

$$+\sum_{m=1}^{M-1}(-1)^m cos(h(2\alpha_M - \alpha_m))] \quad (1)$$

and for an even M,

$$a_h = \frac{4}{h\pi}[\sum_{m=1}^{M}(-1)^{m+1}cos(h\alpha_m)$$
$$+\sum_{m=1}^{M-1}(-1)^{m+1}cos(h(2\alpha_M - \alpha_m))] \quad (2)$$

With b_h=0, by setting a_h=0 up to the desired order $M-1$, $\alpha_m(m=1,...,M-1)$ can be solved from (1) or (2) using nonlinear numerical algorithms such as Newton's methods, with the following condition:

$$0 < \alpha_1 < \alpha_2 < \cdots < \alpha_{M-1} < 30° \quad (3)$$

In this way, the generated switching pattern eliminates harmonics up to the order $M-1$. Another approach [4] is to select chopping angles such that lower harmonics can be attenuated, instead of totally eliminated. This would effectively pushes large harmonics into higher orders, but not without the existence of lower order harmonics.

For a moderate switching frequency, trapezoidal-triangle PWM produces similar waveshape as by the programmed PWM, without the requirement of memory. The PWM gating commands that control the current pattern are generated by comparing a three phase trapezoidal waveform with a triangular carrier waveform. The pattern is controlled by the modulation index and modulation frequency, as in a typical sine-triangular PWM VSI. However, its disadvantage as compared to the harmonic elimination PWM is that the range of modulation index is limited.

For the advanced SVC system presented in this paper, the programmed PWM method is selected for the CSI, with a low switching frequency to eliminate lower order harmonics only. The pre-calculated switching pattern is stored in the EPROM, and is read by the phase-shift control circuit to provide gating signals to the switches.

A closed-loop gating control circuit [3,4] is shown in Fig. 3. In steady-state, the VAR error is zero, thus the switching pattern is read to control the gatings at the phase angle of 90°. The reading frequency is the line frequency, i.e. 60Hz. During transients when the VAR error is not zero, the switching pattern is read to control the gatings at the phase angle different from 90°. This is accomplished by a change in the reading frequency, changing the starting address in the EPROM for the switching pattern to be read. For leading VAR operation, to decrease the reactive power, the reading frequency is increased to decrease the phase angle from negative 90°. For lagging VAR operation, to decrease the reactive power, the reading frequency is decreased to decrease the phase angle from positive 90°.

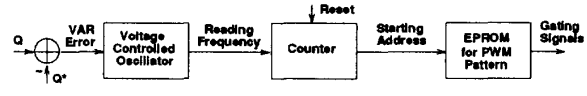

Fig.3 Gating Control Circuit

IV. Operation and Control of VSI

In a SVC using only PWM CSI, a capacitor bank is needed on its ac side, not only to function as a passive filter, but also to make the inverter terminal a voltage source that is needed both for the operation of the CSI and for the interfacing between the CSI and the power network with line inductances. The capacitor bank can be replaced by a PWM voltage source inverter, which then functions as both an active filter and a voltage support.

In order to meet the required filtering characteristics, the harmonic elimination PWM switching [6] can be favorably utilized in the VSI. This is shown in Fig. 4, where α_m denotes angle positions of the chops and M is the total number of harmonics to be eliminated by the PWM VSI. Using quarter-wave symmetry, from Fourier analysis for the output voltage waveform v_a of the VSI, it

can be solved that

$$V_{ah} = \frac{4}{h\pi}[1 + 2\sum_{m=1}^{M}(-1)^m cos(h\alpha_m)] \quad (4)$$

The condition that harmonic current I_{ah} injected into the power network is zero is equivalent to

$$V_{ah} = 0 \quad (5)$$

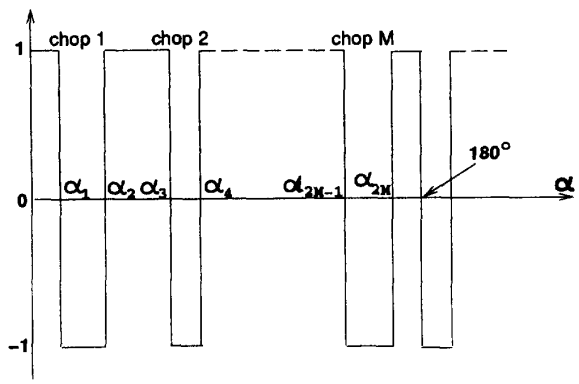

Fig.4 PWM VSI Switching Pattern

From (4) and (5), the angle positions of Fig. 3 can be computed and stored as the PWM VSI switching pattern, eliminating those voltage harmonics such that a short-circuit path, or "sink", is provided to the corresponding current harmonics generated by the CSI.

While the switching pattern of the VSI is fixed, the level of the dc bus voltage needs to be controlled in accordance with the magnitude of the CSI output fundamental current, or the required reactive current. In order that no fundamental component of the CSI current flows through the VSI, the fundamental component of the VSI output voltage is controlled through the dc bus to satisfy, for leading VAR and lagging VAR, respectively,

$$V_{a1} = V_s + \omega L I_{a1} \quad (6)$$

$$V_{a1} = V_s - \omega L I_{a1} \quad (7)$$

Therefore, as a voltage support, the VSI can also be regarded as a separate SVC from the CSI, without suppling fundamental reactive current. Its voltage support operation can be illustrated by the fundamental component phasor diagrams shown in Fig. 5 for leading and lagging VARs. The phase voltage V_{a1} is controlled to be in-phase with respect to the bus voltage V_s, so that the phase current I_{a1} leads or lags V_{a1} by 90°. Relative magnitude of the two voltage phasors V_{a1} and V_s determines the direction of the reactive power.

As with the CSI, the phase angle between the current and phase voltage can not be exactly 90°, since

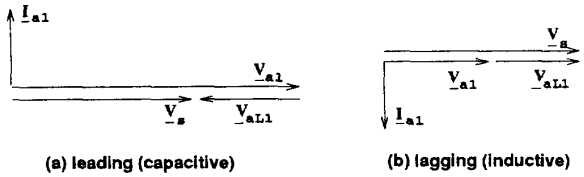

Fig.5 PWM VSI Phasor Diagrams

a small amount of real power is needed to compensate for the switching losses and other losses of the converter; in the meantime, to control the magnitude of the output phase voltage, the level of the dc bus voltage is adjustable by a small shift in the phase angle. The principle and circuit of the phase-shift control is the same as those of the CSI, though a separate design and separate circuit are necessary, since the phase-shift control circuit for the VSI works to shift the phase angle between V_{a1} and V_s around 0°. For leading VAR operation, to decrease the reactive power, this phase angle is shifted to be smaller than 0°, increasing the dc voltage; For lagging VAR operation, to decrease the reactive power, the phase angle is shifted to be smaller than 0°, decreasing the dc voltage.

V. System Design and Integration

The switching frequency for the VSI is selected to be $60 \times 60Hz = 3.6kHz$. Thus the harmonic orders of the output current i_a are greater than 60 with lower order harmonics eliminated. The CSI switching pattern is designed to eliminate 5th order current harmonic with a low switching frequency, thus the lowest order harmonic current through the VSI is 7.

Equivalent circuits for the overall system are shown in Fig. 6(a,b,c), for various harmonic components.

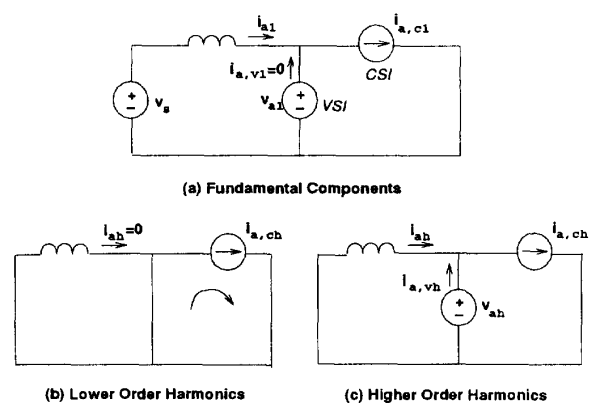

Fig.6 SVC Equivalent Circuits

The size of the ac filter determines the output current smoothness. The output current harmonics of the SVC have been pushed to orders higher than 60th; however, the size of the ac inductor filter is designed to meet further requirements on output current smoothness, measured by the current total distortion factor (THD_i) defined as

$$THD_i = \frac{\sqrt{\sum_{h=61}^{\infty} I_{ah}^2}}{I_{a1}} \tag{8}$$

where

$$I_{ah} = \frac{V_{ah}}{hX_L} \tag{9}$$

From (8) and (9), it can be solved that

$$X_L = \frac{\sqrt{\sum_{h=61}^{\infty} (\frac{V_{ah}}{h})^2}}{THD_i I_{a1}} \tag{10}$$

The ac inductor filter is designed at rated reactive current I_{a1}, which is 1 p.u., with the bus voltage V_s at 1 p.u. For the fixed PWM VSI switching pattern, the voltage harmonics can be calculated after obtaining the fundamental voltage from (6) or (7), for leading VAR or lagging VAR respectively. As studied in [5], for the same amount of reactive power flow, THD_i will be slightly lower for lagging VAR than for leading VAR, therefore the inductor filter should be designed for leading VAR case by using (6).

DC reactors should also be designed to meet requirements on dc ripples. For the CSI, the dc inductor is designed to meet the dc current ripple specification.

From the dc bus current distortion factor

$$THD_i = \frac{\sqrt{\sum_{h=1}^{\infty} I_{dc,ch}^2}}{I_{dc,c}} \tag{11}$$

where

$$I_{dc,ch} = \frac{V_{dc,ch}}{hX_{dc,c}} \tag{12}$$

it can be solved that

$$X_{dc,c} = \frac{\sqrt{\sum_{h=1}^{\infty} (\frac{V_{dc,ch}}{h})^2}}{THD_i I_{dc,c}} \tag{13}$$

For the fixed PWM CSI switching pattern, the dc inductor is designed at rated reactive current for a specified dc current THD_i. The dc bus voltage can be calculated by

$$V_{dc,c} = S_a V_a + S_b V_b + S_c V_c \tag{14}$$

where S_a, S_b and S_c are switching functions for three phases, which are fixed by the switching patterns in steady-state. For example, $S_a = 0$ if both the upper and the lower Phase-A switches are off, $S_a = 1$ if only the upper Phase-A switch is on and $S_a = -1$ if only the lower Phase-A switch is on.

For the VSI, the dc capacitor should be designed to meet the requirement on the dc voltage ripple, using the method analogous to the designing of the dc inductor for the CSI. For the high switching frequency employed for the VSI, the dc voltage ripple tends to be small and negligible even for a small capacitor.

Finally, the parameters for the SVC are listed in the following, including switching patterns for the CSI and the VSI and the sizes of the ac inductor filter and dc inductor and capacitor. The open circuit protection circuit in the CSI is not designed and is neglected in the following simulations.

System parameters:

- CSI switching angles ($M = 2$):
  $\alpha_1 = 18°$.
- VSI switching angles ($M = 20$):
  $\alpha_1 = 2.859°, \alpha_2 = 5.301°, \alpha_3 = 8.618°,$
  $\alpha_4 = 10.645°, \alpha_5 = 14.393°, \alpha_6 = 16.031°,$
  $\alpha_7 = 20.179°, \alpha_8 = 21.459°, \alpha_9 = 25.974°,$
  $\alpha_{10} = 26.933°, \alpha_{11} = 31.779°, \alpha_{12} = 32.459°,$
  $\alpha_{13} = 37.603°, \alpha_{14} = 38.049°, \alpha_{15} = 43.469°,$
  $\alpha_{16} = 43.728°, \alpha_{17} = 49.455°, \alpha_{18} = 49.580°,$
  $\alpha_{19} = 55.956°, \alpha_{20} = 56.004°.$
- AC inductor filter: $X_L = 0.27 p.u.$ for $THD_i \leq 5\%$.
- DC inductor for CSI: $X_{dc,c} = 1.35 p.u.$ for dc current $THD_i \leq 5\%$.
- DC capacitor for VSI: $X_{dc,v} = 1.20 p.u.$ for dc voltage $THD_v \leq 5\%$.

VI. Computer Simulations

Switching patterns of the CSI and the VSI are shown in Fig. 7.

For a SVC output reactive current $I_{a1} = 1 p.u.$, leading VAR operation is simulated and the results are shown in Fig. 8 through Fig. 10. Fig. 8(a,b) show the output current and dc current waveforms of the CSI. Fig. 9(a,b) show the overall output current of the SVC and current through the VSI active filter. Fig. 10(a,b) show the output phase voltage and dc bus voltage of the VSI. For the output current in Fig. 9(a), $THD_i = 5.1\%$; For the dc current of the CSI in Fig. 8(b), $THD_i = 5.2\%$; For the dc voltage of the VSI in Fig. 10(b), $THD_v = 2.8\%$.

For a SVC output reactive current $I_a = 1 p.u.$, lagging VAR operation is simulated and the results are

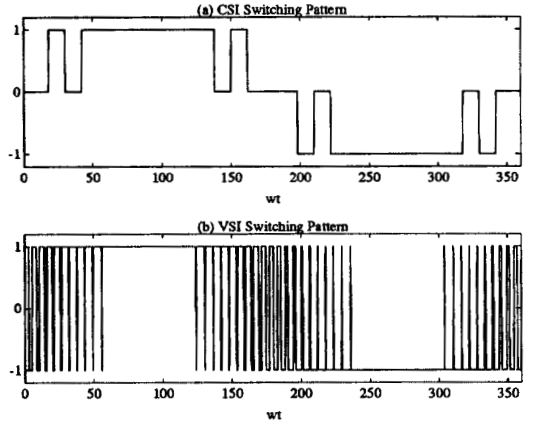

Fig.7 Fixed Harmonic-Elimination Switching Patterns

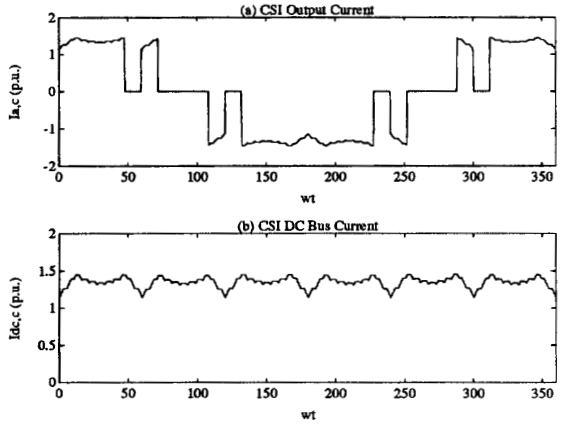

Fig.8 CSI Currents for Leading VAR ($I_{a1} = 1p.u.$)

shown in Fig. 11 through Fig. 13. Fig. 11(a,b) show the output current and dc current waveforms of the CSI. Fig. 12(a,b) show the overall output current of the SVC and current through the VSI active filter. Fig. 13(a,b) show the output phase voltage and dc bus voltage of the VSI. For the output current in Fig. 12(a), $THD_i = 4.6\%$; For the dc current of the CSI in Fig. 11(b), $THD_i = 2.8\%$; For the dc voltage of the VSI in Fig. 13(b), $THD_v = 5.1\%$.

Fig. 14 shows a simulation of the phase-shift control of the reactive power for a change of leading reactive current from $1p.u.$ to $0.333p.u.$ A phase-shift of the CSI also results in a decrease in its dc and ac currents. Coordinated designing of the phase-shift controllers for the VSI and the CSI is necessary, such that during transients, the VSI draws small or no fundamental current component.

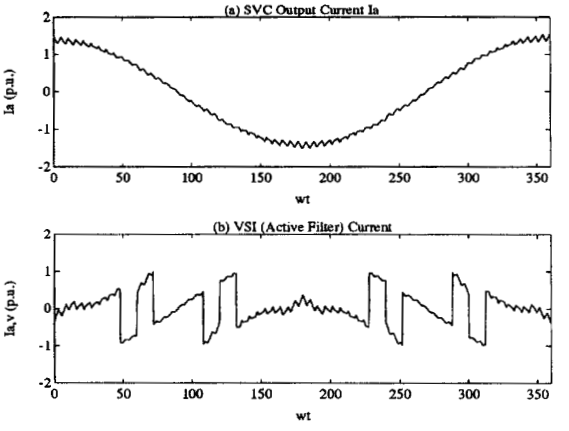

Fig.9 SVC Output Current and VSI Current for Leading VAR ($I_{a1} = 1p.u.$)

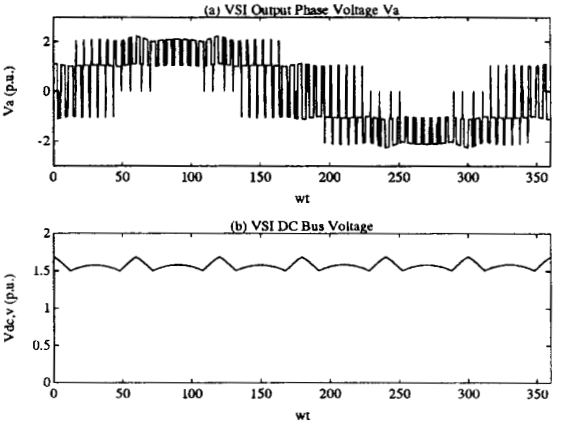

Fig.10 VSI AC and DC Voltages for Leading VAR ($I_{a1} = 1p.u.$)

VII. Conclusions

An advanced reactive power compensator has been presented, for both power system control applications and high power utility applications. The new system attempts to resolve the usual confliction between power converter switching losses and harmonic distortions. Even though a detailed performance analysis is yet to be done, it has been shown through the preliminary design and computer simulation that the system can achieve high performance via systemized and coordinated designing. The use of two converters, i.e. a VSI and a CSI, can be justified by the reduction in reactor and passive filter sizes, and simplicity in control with additional flexibility.

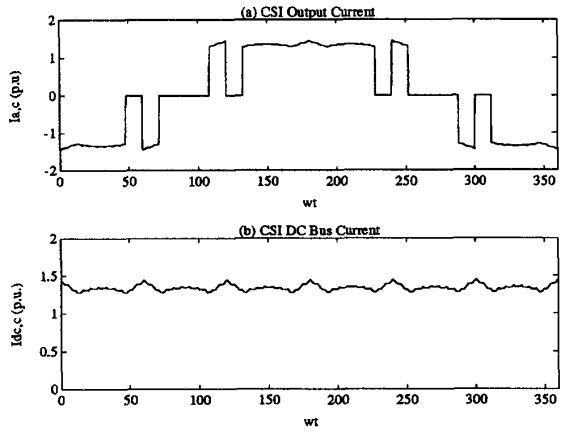

Fig.11 CSI Currents for Lagging VAR ($I_{a1} = 1p.u.$)

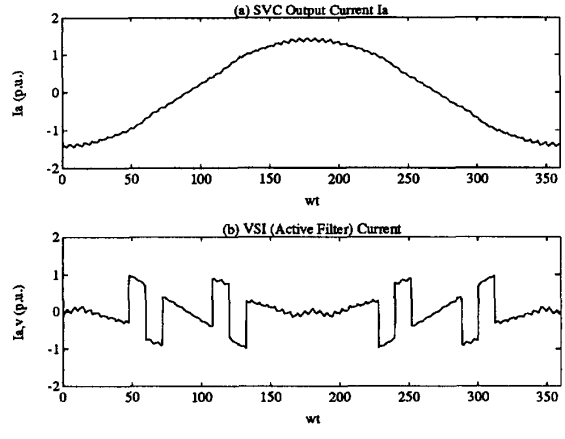

Fig.12 SVC Output Current and VSI Current for Lagging VAR ($I_{a1} = 1p.u.$)

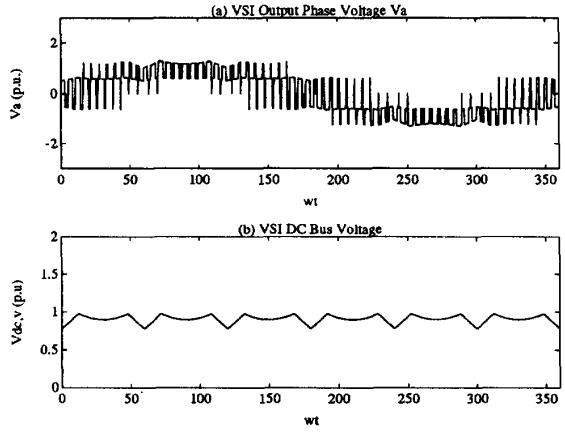

Fig.13 VSI AC and DC Voltages for Lagging VAR ($I_{a1} = 1p.u.$)

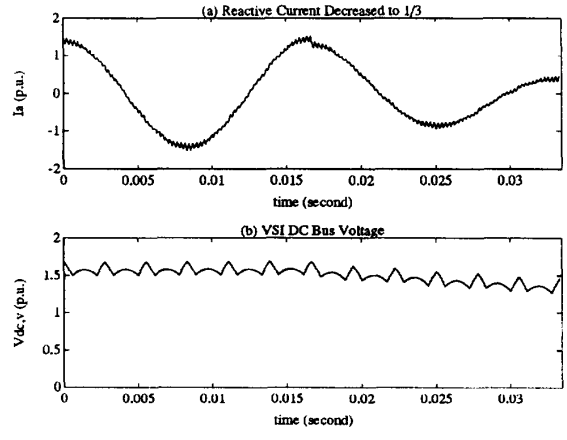

Fig.14 Dynamics for Leading VAR

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