AlGaN/GaN HEMTs on SiC With f_T of Over 120 GHz

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***Abstract*—AlGaN/GaN high electron mobility transistors (HEMTs) grown on semi-insulating SiC substrates with a 0.12 μm gate length have been fabricated. These 0.12-μm gate-length devices exhibited maximum drain current density as high as 1.23 A/mm and peak extrinsic transconductance of 314 mS/mm. The threshold voltage was −5.2 V. A unity current gain cutoff frequency (f_T) of 121 GHz and maximum frequency of oscillation ($f_{\max}$) of 162 GHz were measured on these devices. These f_T and $f_{\max}$ values are the highest ever reported values for GaN-based HEMTs.**

***Index Terms*—GaN, high electron mobility transistors (HEMTs), SiC.**

I. Introduction

GaN-BASED high electron mobility transistors (HEMTs) are excellent candidates for high power and high frequency applications at elevated temperatures [1]–[3]. This is due to the advantageous material properties such as wide bandgap (3.4 eV of GaN to 6.2 eV of AlN) leading to high breakdown fields (1–3 $\times 10^6$ V/cm), high saturated-electron drift velocity (2.2×10^7 cm/s), and the existence of AlGaN/GaN heterostructure with high conduction band offset and high piezoelectricity resulting in high sheet carrier densities in the 1.0×10^{13} cm^{-2} range. Recently, tremendous progress has been recorded in the material quality and device processing of GaN-based HEMTs. These have resulted in significant improvements in the dc and RF performances of these devices and new record performance are continuously being reported. A breakdown voltage of as high as 570 V in an AlGaN/GaN HEMT with a source-drain spacing of 13 μm and a gate length of 0.5 μm using an overlapping gate structure was reported recently [4]. AlGaN/GaN HEMTs with current density of 1.7 A/mm have also been reported [5]. Though power density as high as 10.7 W/mm at 10 GHz has been achieved on GaN-based devices yet their suitability for power applications at frequencies $>$ 30 GHz is currently being limited by the speed of these devices [6]. Recently, AlGaN/GaN HEMTs with record unity current gain cutoff frequency (f_T) 110 GHz and maximum frequency of oscillation ($f_{\max}$) over 140 GHz have been demonstrated by reducing the gate length down to 50 nm [7]. However, this reduction of gate length leads to lowering of breakdown voltage [8]. In this letter, we present our results on 0.12 μm gate length AlGaN/GaN HEMTs on SiC substrates. These 0.12 μm gate-length devices exhibited current density of 1.23 A/mm, peak transconductance of 314 mS/mm, gate-drain breakdown voltage of over 60 V, a record high f_T of 121 GHz, and $f_{\max}$ of 162 GHz.

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II. Device Structure and Fabrication

The layer used in the present study was grown on semi-insulating (0001) 4H-SiC substrates by metal-organic chemical vapor deposition (MOCVD). The epilayer consists of a 100-nm AlN buffer, 2-μm undoped GaN, a 5-nm undoped $Al_{.25}Ga_{.75}N$ spacer, a 10-nm Si-doped ($\sim 5 \times 10^{18}$ cm^{-3}) $Al_{.25}Ga_{.75}N$ charge supply layer, and a 10-nm undoped $Al_{.25}Ga_{.75}N$ barrier layer. We also had a low-level flux of trimethylindium (TMI) present during the growth of all the layers of the structure. As reported before, the presence of the indium surfactant helps in improving the surface and interface roughness by incorporation of trace amounts of indium [9]. Hall measurements showed a sheet carrier concentration of 1.1×10^{13} cm^{-2} and an electron mobility of 1300 cm^2/volt-s at room temperature on as-grown wafers. The structures grown at zero level of TMI flux on average exhibit 2-DEG mobility that is 10–20% lower than those grown with TMI flux. The reduction of the surface and interface roughnesses of heterostructures brought about by the addition of TMI flux also results in the improvement of the current lag caused by carrier trapping. A brief summary of the results of a comparative study of HEMT structures grown with and those without TMI flux are shown in Table I.

For the present work, the first step for the device fabrication was mesa-isolation using Cl_2/Ar plasma in an inductively-coupled-plasma reactive ion etch (ICP-RIE) system. Next, ohmic contacts were formed by rapid thermal annealing of evaporated Ti/Al/Ti/Au at 840°C for 30 s in N_2 ambient. A pretreatment of the ohmic contact area using $SiCl_4$ plasma in a RIE was performed prior to Ti/Al/Ti/Au metallization [10]. Using on-wafer transfer length method (TLM) patterns, the ohmic contact resistance was typically measured to be $\sim$ 0.35 Ω-mm. T-shaped gates with gate lengths (L_g) of 0.12, 0.15 and 0.25 μm were defined using a trilayer PMMA/P(MMA-MAA)/PMMA and electron-beam lithography. Ni/Au metals were then evaporated for gate metallization. The gates were centered within the drain-source. Overlay metallization on ohmic contacts and measurement pads was also deposited during gate formation. The devices had a gate width of 100 μm and a source-drain spacing of 2 μm.

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TABLE I
COMPARISON OF HEMT STRUCTURES GROWN WITH AND THOSE WITHOUT TMI FLUX

Parameter	TMI flux = 0	TMI flux > 0
Surface roughness (Å)*	5-7	2-4
Electron mobility (cm^2/volt-sec)	1050-1100	1250-1350
Pulsed/DC current ratio**	0.45-0.75	0.85-1.0

*The RMS surface roughness was measured over 5 × 5 μm^2 area using AFM.

**The pulsed drain current was measured after the gate voltage pulse returns to zero bias from the value of around threshold voltage. DC drain current was measured at zero gate bias.

III. RESULTS AND DISCUSSION

The dc measurements were carried out using an HP4145B semiconductor parameter analyzer. Shown in Fig. 1 is the typical drain current-voltage (I_D–V_{DS}) characteristics of a 0.12 μm gate-length device. The gate was biased from -8 V to 2 V in a step of 2 V. The devices exhibited a maximum drain current density of 1.23 A/mm at a gate bias of 2 V and a drain bias of 15 V. The device pinched off completely at $V_{gs} = -8$ V, with drain current as low as 0.66 mA/mm at $V_{ds} = 10$ V and 3.5 mA/mm at $V_{ds} = 15$ V. The knee voltage is less than 5.0 V. No drop in drain current was observed at drain biases up to 15 V, indicating the effectiveness of the i-SiC in removing the channel heat resulting from high current density. The saturation current I_{dss} is about 1.09 A/mm at 15 V. The dc transfer characteristics are shown in Fig. 2. The drain was biased at 8 V. A peak extrinsic transconductance (g_m) of 314 mS/mm was measured at $V_{gs} = -3.9$ V. By defining the threshold voltage (V_{th}) as the gate bias intercept of the extrapolation of drain current at the point of peak g_m, the V_{th} was determined to be -5.2 V. The off-state gate-drain breakdown voltage of > 60 V was measured at a gate current density of 1 mA/mm.

RF measurements were carried out on-wafer using a Casacade Microtech Probe and an HP8510B network analyzer in the 1–40 GHz range. The effect of pad parasitics were de-embedded by conventional Y parameter subtraction. Fig. 3 shows the short-circuit current gain ($| h_{21} |$) and maximum stable gain/maximum available gain (MSG/MAG) derived from on-wafer S-parameter measurements as a function of frequency for the 0.12 μm gate-length device. The values of unity current gain cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) were determined by extrapolation of the $| h_{21} |$ and MSG data at -20 dB/decade. At a drain bias of 8 V and a gate bias of -3.95 V, an f_T of 121 GHz and an f_{max} of 162 GHz were obtained, which to the best of the authors' knowledge are the highest data ever reported for GaN-based HEMTs. The extrinsic f_T and f_{max} values were 102 GHz and 133 GHz, respectively. This high rf performance is attributed to the high quality of material and also to the optimized device processing. A plot of f_T as a function of L_g is shown in the inset of Fig. 3. As seen, f_T increases steadily with decreasing L_g. The

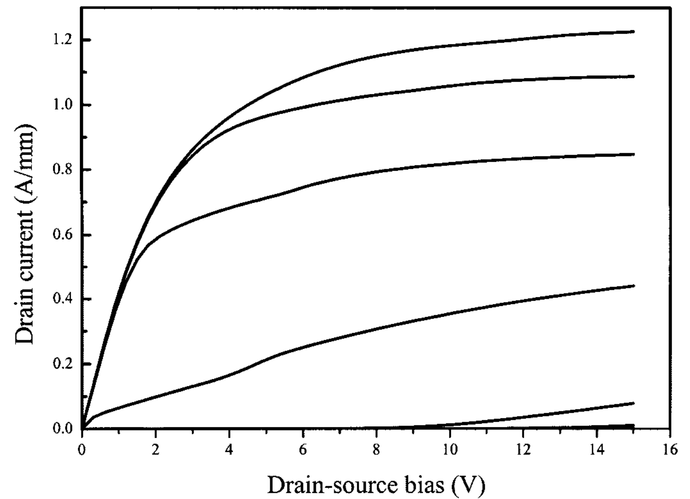

Fig. 1. Drain current-voltage (I_D–V_{DS}) characteristics of a 0.12 μm× 100 μm AlGaN/GaN HEMT on SiC substrate. The gate bias was swept from -8 to 2 V in a step of 2 V.

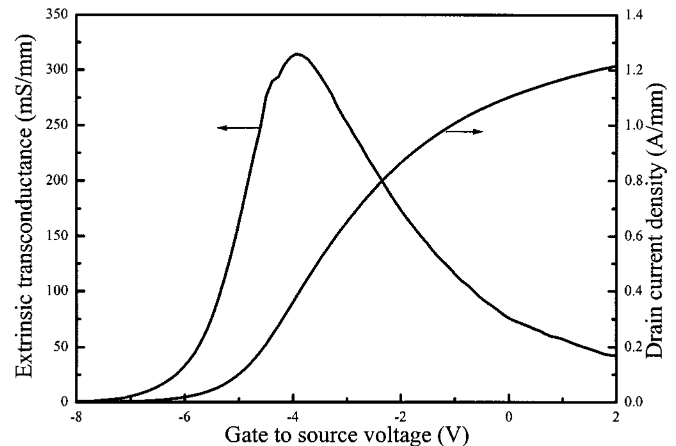

Fig. 2. Transfer characteristics of the 0.12 μm× 100 μm AlGaN/GaN HEMT on SiC substrate. The drain bias was 8.0 V.

value of f_T ranged from 66 GHz for the 0.25 μm to 121 GHz for 0.12 μm. The effective electron velocity (v_{eff}) under the gate was estimated from the dependence of f_T on gate length using a simple expression from the charge current model : $f_T = v_{eff}/2\pi L_g$ [11]. We estimate v_{eff} to be $\sim 9 \times 10^6$ cm/s.

The variation of f_T and f_{max} as a function of drain current density is shown in Fig. 4. In these measurements the drain was biased at 8.0 V, while the gate was biased between -5.5 V and 0. The drain current was in the range of 53 mA/mm to 1.026 mA/mm. The f_T values varied from 35 GHz to 121 GHz while f_{max} ranged from 66 to 162 GHz. At lower drain current, f_T increases with a increase in drain current due to increase in transconductance. The peak f_T is measured at a drain current of 370 mA/mm where the peak g_m is located. Further increase in drain current results in a drop of f_T due to the reduction of g_m at higher drain current as C_{gs} weakly depends on the gate bias. It is worth noting that the device still exhibits f_T and f_{max} of over 60 GHz even at $I_{ds} = I_{dss}$ ($V_{gs} = 0$ V), which indicates the potential for high power at high frequencies.

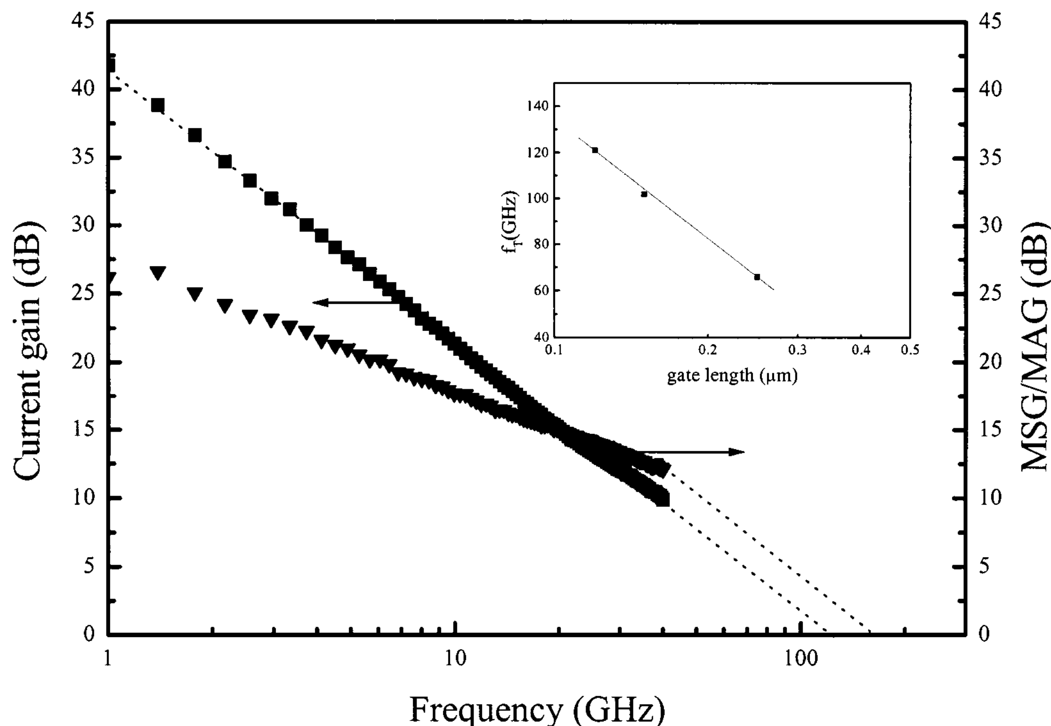

Fig. 3. Short-circuit current gain (| h_{21} |) and maximum stable/maximum available gain (MSG/MAG) of a 0.12 μm× 100 μm AlGaN/GaN HEMT on SiC substrate. The device was biased at $V_{\rm ds} = 8$ V and $V_{\rm gs} = -3.95$ V. Inset: Unity current gain cutoff frequency versus gate length.

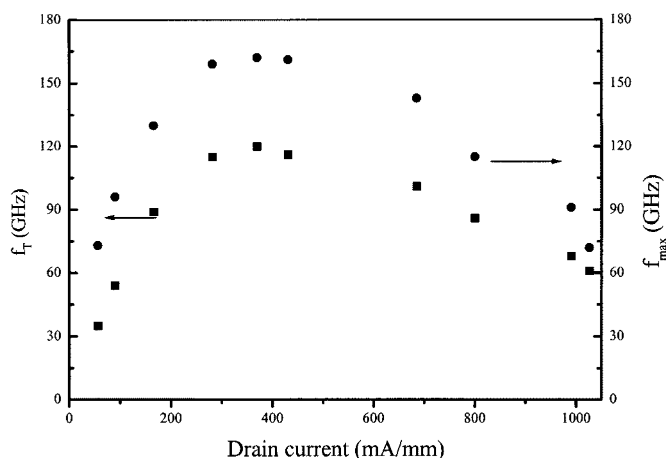

Fig. 4. Unity current gain cutoff frequency (f_T) and maximum frequency of oscillation ($f_{\rm max}$) versus drain current for a 0.12 μm× 100 μm AlGaN/GaN HEMT on SiC substrate.

IV. Conclusion

We have demonstrated excellent high-frequency performance of AlGaN/GaN HEMTs on a semi-insulating SiC substrate. An f_T value as high as 121 GHz, an $f_{\rm max}$ value as high as 162 GHz, a transconductance of 314 mS/mm, and current density of 1.23 A/mm were obtained for 0.12 μm gate-length devices. Continued improvements in AlGaN/GaN heterostructure material quality combined with advances in processing should lead to devices with even better performances.

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