Analytical Model for Power Switching GaN-Based HEMT Design

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***Abstract*—The GaN high-electron mobility transistor (HEMT) structure has been widely investigated, particularly for radio-frequency applications. This structure is suitable for high-frequency switching applications in power electronics because of the high breakdown field of GaN and the high mobility of the channel. In this paper, a physical model for predicting the power-switching operation of GaN-based HEMTs as a function of material and device parameters is proposed. Analytical equations for total losses and power dissipation density are derived and discussed both qualitatively and quantitatively.**

***Index Terms*—Analytical model, GaN high-electron mobility transistor (HEMT), power switching.**

I. Introduction

HIGH POWER density [1], [2] and very high performance in various power electronics applications [3]–[7] have been demonstrated for GaN high-electron mobility transistors (HEMTs), and GaN technology is a promising candidate for many radio frequency (RF) applications. In the case of power-switching applications, GaN devices promise lower ON-state and switching power dissipation than other technologies, enabling a new class of high-performance power electronics. From a technological point of view, many solutions have been already proposed to overcome the main limitations affecting the microwave power behavior of GaN HEMTs. The introduction of SiN_x passivation, as first demonstrated by Green *et al.* [8] and well assessed later on, solves the direct current (dc)-to-RF dispersion. Moreover, the optimization of the field-plate structure addresses the dynamic ON-resistance increase during a high-voltage operation, as reported by Saito *et al.* [9], and the breakdown performance, as reported by Dora *et al.* [10]. The combination of all these solutions has already enabled highly efficient GaN HEMT power operation [7]. However, relatively less work has been done to develop quantitative physical models for transistor performance for power-switching applications.

The reduction of the ON-state resistance and the increase in the breakdown voltage are key factors for power-switching operation. These two parameters are typically used while estimating the figure of merit while comparing the performance of either different device structures or different materials. Detailed models exist for estimating these parameters in power devices based on silicon. However, because of the very high power capability of GaN HEMTs, the design and analysis of the power-switching behavior cannot rely only on ON-state resistance and breakdown voltage but also have to take into account the actual power capabilities of both material and device's structure. For this reason, all previous models, mostly based on Baliga's analysis, are not able to estimate the GaN HEMTs power behavior.

In the case of the lateral HEMT device, the design of power-switching transistor would proceed as follows. First, depending on the breakdown field, the length of the drift region and the charge density are chosen. Once these are selected, the optimal width $W_{\rm opt}$ of the device can be determined by minimizing the total power dissipation since the resistive losses are proportional to $1/W_{\rm opt}$, and the switching losses are proportional to $W_{\rm opt}$. Such an analysis was carried out by Saito *et al.* [11] for GaN and diamond devices and was very helpful in laying out a detailed quantitative estimation of power device performance.

However, the device models developed earlier have not addressed certain issues that are pertinent to GaN power-switching devices in a satisfactory way. First, the current carrying capacity of the device is not taken into account. As the frequency of operation is increased and "optimal" device width $W_{\rm opt}$ reduces, the device may not actually be able to support the current specified. The model we present here provides a physical relationship between the current capacity, carrier density, and device width.

Second, although devices based on wide-band-gap materials such as GaN provide lower total power loss due to the higher breakdown field, the thermal dissipation density in wide-band-gap devices is significantly higher ($10\times$ or more) than comparable silicon devices. Simply put, the higher breakdown fields allow smaller device dimensions and hence lead to lower total loss but higher power dissipation density. However, the thermal conductivity of GaN is similar to silicon, and thermal constraints are therefore expected to play a very important role in the design of these devices. In our model, we therefore

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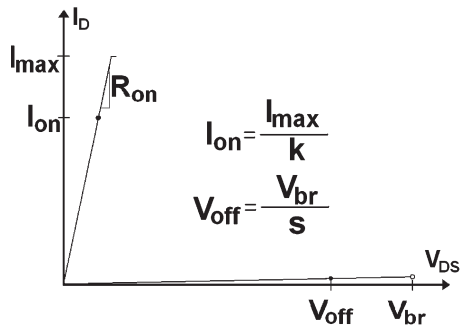

Fig. 1. Simplified I–V characteristic for switching operation.

provide built-in parameters so that the device design can be carried out with regard to thermal considerations.

The overall objective of this paper is to provide a design path for a device with given parameters (maximum voltage and current). We note that since our model is based on physical parameters related to the material only, the design maintains some universality and may be applied to different device geometry and materials (such as diamond and AlGaN).

II. Analytical Model

The nonideal behavior of an electron device operating as a switch is reported in terms of conduction and switching losses. The main sources of conduction losses are the ON-state nonzero voltage, due to the ON-state resistance, and the OFF-state nonzero current, due to leakage effects. The switching losses are due to charging of capacitors associated with the device.

The schematic I_d–V_{ds} characteristic, limited to the switching operation, is depicted in Fig. 1. In our analysis, we consider the actual I–V switching operating points $(V_{\rm off}, I_{\rm on})$ different from their limit values, i.e., $V_{\rm br}$ and $I_{\rm max}$, respectively. As shown in Fig. 1, $V_{\rm br}$ is assumed to be s times higher than $V_{\rm off}$ and $I_{\rm max}$ k times higher than $I_{\rm on}$.

Fig. 2 reports the proposed process flow for the device designing. Starting from the total power specification in terms of the I–V operating points $(V_{\rm off}, I_{\rm on})$, the device design flows through the breakdown voltage and maximum current specifications $(V_{\rm br}, I_{\rm max})$. Then, sheet charge concentration, mobility, and device geometry (n_s, μ, W_g, L_{gd}) are chosen according to power density constraints and minimization of the total losses.

In the following, all the parameters and constants adopted in our model are summarized.

A. Key Parameters and Constants

μ 2-D electron gas (2-DEG) channel mobility, expressed in $\rm cm^2/V \cdot s$;
q electron unit charge, expressed in 1.6×10^{-19} C;
n_s sheet charge density, expressed in $\rm cm^{-2}$;
$\varepsilon_{\rm GaN}$ GaN dielectric constant, expressed in 8.411×10^{-13} F/cm;
$\omega_{\rm op}$ GaN optical phonon angular frequency, expressed in 1.367×10^{14} Hz;

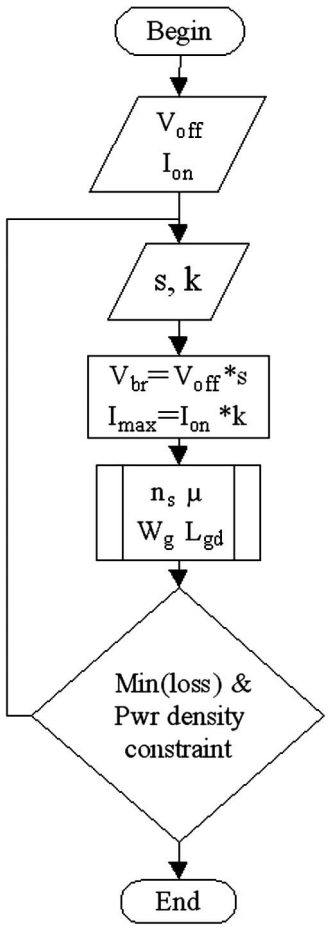

Fig. 2. Proposed process flow for device designing.

k, s I–V operating points coefficients, respectively, for drain current and drain-to-source voltage;
$f_{\rm sw}$ switching frequency, expressed in hertz;
D duty cycle;
x_d gate-to-drain depletion region extension in the gate-to-drain access region, expressed in cm;
E_c critical electric field, expressed in megavolts per centimeter;
L_{sd} source-to-drain spacing, expressed in centimeters;
L_{gd} gate-to-drain spacing, expressed in centimeters;
L_{sg} source-to-gate spacing, expressed in centimeters;
W_g gate width, expressed in centimeters;
L_g gate length, expressed in centimeters;
R_s source contact resistance, expressed in ohms;
R_d drain contact resistance, expressed in ohms;
$R_{\rm on}$ ON-state resistance, expressed in ohms;
$R_{\rm sh}$ sheet resistance, expressed in ohms per square;
$I_{\rm max}$ maximum drain current density, expressed in amperes per millimeter;
$I_{\rm on}$ ON-state-switch drain current, expressed in amperes;
$I_{\rm off}$ OFF-state-switch drain current at $V_{\rm off}$, expressed in amperes;
$V_{\rm br}$ breakdown voltage, expressed in volts;
$V_{\rm off}$ OFF-state-switch drain-to-source voltage, expressed in volts;

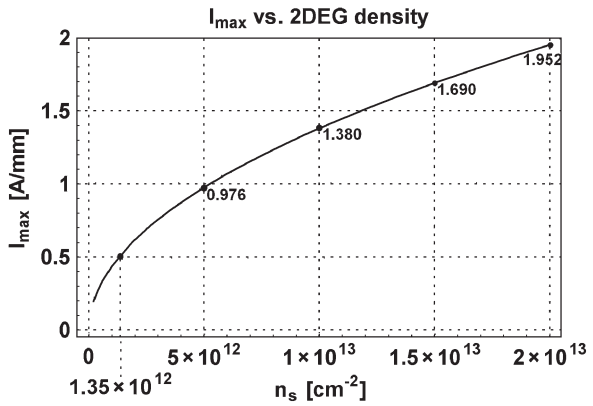

Fig. 3. Maximum drain current density as the function of the 2-DEG density.

C_{gd} gate-to-drain capacitance, expressed in farad;
Q_{gd} gate-to-drain capacitor stored charge, expressed in coulomb.

B. I–V Operating Points and Device Geometry

According to the device physics, the relation between the I–V operating points and device geometry can be derived by considering the 2-DEG carrier concentration and the gate width for $I_{\rm on}$ and the critical electric field and the gate-to-drain spacing for $V_{\rm off}$. In our model, the expression of the maximum drain current density, as reported in (1), is given by a Fermi circle analysis, to be published elsewhere [12], i.e.,

$$I_{\max} = \frac{q\omega_{\rm op}\sqrt{n_s}}{\sqrt{8\pi}}. \tag{1}$$

Using (1), the maximum drain current density is plotted in Fig. 3 as a function of the 2-DEG charge concentration. As pointed out in [12], this equation fits the experimental data well.

An exact calculation of the breakdown voltage would involve charge density, gate-to-drain spacing, and GaN critical electric field. However, Wemple *et al.* [13] and Hikosaka *et al.* [14] have reported on the relationship between the breakdown voltage and sheet charge density for planar structures such as HEMT and metal–semiconductor field-effect transistor. In [15] and [16], a linear relationship between the breakdown voltage and the gate-to-drain spacing was observed. In this paper, it was shown that when the 2-DEG in the gate-to-drain access region is completely depleted, the depletion region hits the drain contact. From this point on, the maximum electric field linearly increases, and breakdown occurs. The critical electric field for GaN has been determined to be close to 1 MV/cm—ranging from 0.8 MV/cm [16] to approximately 1.4 MV/cm [15]—assuming a linear relationship between the depletion region extension in the gate-to-drain access region x_d and the breakdown voltage $V_{\rm br}$. We note that the experimental critical electric field, as reported in [15] and [16], is lower than the critical value for GaN (3.3 MV/cm). While this may be partially attributed to a nonuniform field in the depletion region, the phenomenon of soft breakdown in AlGaN/GaN lateral structures is still not completely understood. In this paper, we will use this experimental result in our modeling.

Using (1) and given the assumption of a constant electric field distribution across the gate-to-drain depleted region, the relationships between the device geometry (L_{gd}, W_g) and the I–V operating points $(I_{\rm on}, V_{\rm off})$ can be derived as

$$W_g = \frac{I_{\rm on}}{(I_{\max}/k)} = kI_{\rm on}\frac{\sqrt{8\pi}}{q\omega_{\rm op}\sqrt{n_s}} \tag{2}$$

$$L_{gd} = \frac{V_{\rm off}}{(E_c/s)} = sV_{\rm off}\frac{1}{E_c}. \tag{3}$$

As pointed out in (2) and (3), the introduction of the coefficients k and s into the definition of $I_{\rm on}$ and $V_{\rm off}$ (see Fig. 1) directly translates into the device geometry definition. As addressed later in this paper, this will give to the designer one more degree of freedom for loss minimization and power density optimization. The current parameter k defines the normal operating parameters of the device. Under abnormal conditions, such as a short circuit, the maximum current passing through the transistor will be higher and limited by the intrinsic current carrying capacity of the transistor. We note that the short-circuit performance is of critical importance in a practical design of power devices.

C. Conduction and Switching Losses

The device ON-state resistance can be divided into three main components: the sheet resistance $R_{\rm sh} = (q\mu n_s)^{-1}$ and the source and drain contact resistances (R_s and R_d, respectively). For a 2-DEG channel, the ON-resistance can be expressed as

$$R_{\rm on} = \frac{L_{sd}}{W_g}R_{\rm sh} + R_s + R_d = \frac{L_{sd}}{W_g q\mu n_s} + R_s + R_d. \tag{4}$$

For the high-voltage transistors considered here (with $L_{sd} \sim 10\ \mu$m), we expect that the contribution of the contact resistances R_s and R_d is smaller than that of the sheet resistance, and their contribution will be neglected. Since for power-switching devices the gate-to-drain spacing is much higher than the gate-to-source one, in the following, the L_{sd} term, as reported in (4), will be replaced by L_{gd}.

Based on the ON-state resistance and L_{gd} expressions [(4) and (3), respectively], the ON-state and OFF-state dc power dissipation can be derived as

$$P_{\rm dc\_on} = I_{\rm on}^2 R_{\rm on} \cong \frac{s}{k} I_{\rm on} V_{\rm off} \frac{\omega_{\rm op}}{E_c \mu\sqrt{8\pi}\sqrt{n_s}} \tag{5}$$

$$P_{\rm dc\_off} = V_{\rm off} I_{\rm off}. \tag{6}$$

In summary, the total dc power dissipation, also known as conduction losses, can be expressed as

$$P_{\rm diss\_dc} \cong d\frac{s}{k}\frac{I_{\rm on}V_{\rm off}\omega_{\rm op}}{E_c\mu\sqrt{8\pi}\sqrt{n_s}} + (1-d)V_{\rm off}I_{\rm off}. \tag{7}$$

The adopted model for the switching losses calculation is depicted in Fig. 4. In this model, the charge and discharge of the gate-to-drain capacitor is taken into account. In the gate-to-drain reverse bias condition, the modulation of the depletion region width x_d during the switching operation corresponds to charging and discharging the C_{gd}.

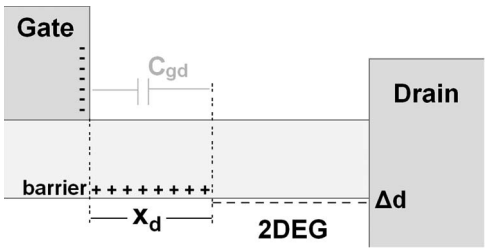

Fig. 4. Adopted model for the switching losses calculation.

According to our breakdown analysis [as summarized by (3)], the depletion region extension, as function of the OFF-state voltage, can be derived as

$$x_d \propto \frac{V_{\rm off}}{E_c}. \tag{8}$$

Because of the discrepancy between the experimental critical field E_c and its theoretical limit, (8) can be associated to a best case scenario if the theoretical limit is adopted. As previously mentioned, this best case scenario can be assumed to be valid if multiple-field plates and cap-layer engineering are involved in order to get a good control of the electric field profile across the depleted region—in both magnitude and distribution. In our calculation, a realistic critical electric field value, close to the experimental observations, will be involved.

The switching losses depend on the switching frequency and the switching time. In our model (see Fig. 4), the switching time depends on the time during charge or discharge of the gate-to-drain capacitor. Under the assumption of hard gate driving, the stored charge is simply the product between the gate-to-drain current and the switching time. Therefore, using (8), the switching power dissipation can be evaluated as

$$P_{\rm diss\_sw} = V_{\rm off} Q_{gd} f_{\rm sw} = V_{\rm off} q n_s x_d W_g f_{\rm sw}. \tag{9}$$

Combining (8) and (2), the switching dissipation is obtained as [see (10)]

$$P_{\rm diss\_sw} \propto k I_{\rm on} V_{\rm off}^2 f_{\rm sw} \frac{\sqrt{n_s}\sqrt{8\pi}}{E_c \omega_{\rm op}}. \tag{10}$$

We note that while switching losses linearly increase as the frequency increases, overall gains may be made at the system level as passive component sizes are reduced.

Using (7) and (10), the overall power dissipation $P_{\rm diss}$, neglecting the OFF-state dc power dissipation can be expressed as

$$P_{\rm diss} \cong d\frac{s}{k}\frac{I_{\rm on} V_{\rm off} \omega_{\rm op}}{E_c \mu \sqrt{8\pi}\sqrt{n_s}} + k I_{\rm on} V_{\rm off}^2 f_{\rm sw} \frac{\sqrt{n_s}\sqrt{8\pi}}{E_c \omega_{\rm op}}. \tag{11}$$

Apart from constants and material parameters, the following four different terms can be identified in the total power dissipation expression.

1) $I_{\rm on}$ and $V_{\rm off}$—The dc power dissipation is directly proportional to the total switching power, but switching losses are proportional to $I_{\rm on} V_{\rm off}^2$.
2) Two-dimensional electron gas charge density and mobility—High charge density and mobility have to be achieved in the 2-DEG in order to get low dc power dissipation. However, in the case of switching losses, dissipation increases as the charge density is increased.
3) s—According to (3), higher back-off from the breakdown condition means higher gate-to-drain distance, thus, higher resistivity of the active channel [see (4)].
4) k—higher k (and higher W_g) lead to a reduction in the ON-state losses but increase in the switching losses.

Although the total losses are linearly dependent on $I_{\rm on}$ [see (11)], the predicted efficiency is not. Additionally, the efficiency decreases as the maximum OFF-state voltage is increased.

D. Power Density Constraint

The analytical expression of the power dissipation density can be derived, as in (12), by dividing the total power losses [see (11)] by the active area of the device using (2) and (3), i.e.,

$$P_{\rm diss\_dens} \cong \frac{1}{k^2}\frac{1}{\mu}\frac{q d \omega_{\rm op}^2}{8\pi} + \frac{1}{s} q n_s V_{\rm off} f_{\rm sw}. \tag{12}$$

Consideration of both total losses [see (11)] and power dissipation density [see (12)] will play a dominant role in the device design. In our model, for a given total switching power and a given structure, i.e., given 2-DEG charge and mobility, the power dissipation density can be addressed by means of the coefficients k and s, according to the losses minimization.

The areal thermal dissipation (as well as the total losses) is a very critical parameter while designing power-switching devices. In [7], with an efficiency of 97.8% at 300-W output power, the power dissipation density is approximately 1.8 kW/cm^2. Operating the device at high power dissipation density, requires a careful analysis of the heat dissipation capability. Moreover, long-term reliability issues have to be considered.

In the following section, the proposed model will be quantitatively discussed through examples involving typical device specifications.

III. Quantitative Modeling

In this section, we apply the model developed here to determine the parameters for several test cases. As proposed in Fig. 2, the first specification is the total switching power, in terms of ON-state and OFF-state operation points. In the first case, we assume $V_{\rm off} = 500$ V and $I_{\rm on} = 1.5$ A for a total power of 750 W and a switching frequency of 1 MHz. Based on (3), for a critical electric field of 1.5 MV/cm and $s = 3$, L_{gd} is 10 μm. Fig. 5 reports the switching efficiency as a function of k, thus W_g [see (2)], for three different values of $n_s = 4 \times 10^{12}$, 8×10^{12}, and 1.5×10^{13} cm^{-2}. As shown, a theoretical maximum efficiency of 99.9% can be obtained for the highest simulated charge density, i.e., 1.5×10^{13} cm^{-2}, for k approximately 11 ($W_g \sim 9.8$ mm). The total active area of the device, as a product between L_{gd} and W_g, as previously obtained, is 0.098 mm^2 or 98×10^{-5} cm^2. The resulting power dissipation density is approximately 765 W/cm^2. Assuming

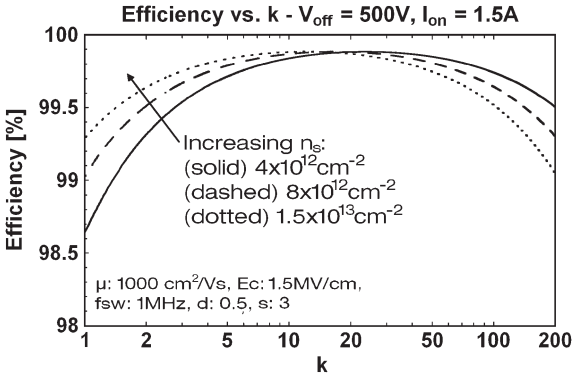

Fig. 5. Switching efficiency as the function of k for three different carrier densities of 4×10^{12}, 8×10^{12}, and 1.5×10^{13} cm^{-2}. The most important simulated parameters are reported.

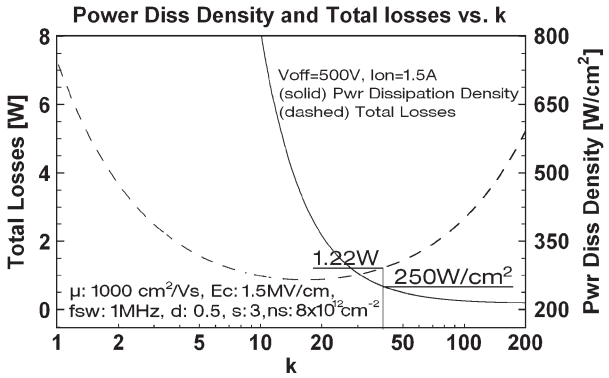

Fig. 6. Power dissipation density and total losses as the function of k for a carrier density of 8×10^{12} cm^{-2}. The simulated case is the same as in Fig. 5. The most important parameters are reported.

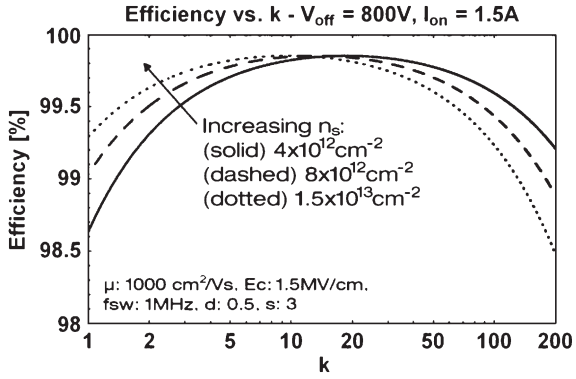

Fig. 7. Switching efficiency as the function of k for three different carrier densities of 4×10^{12}, 8×10^{12}, and 1.5×10^{13} cm^{-2}. The most important simulated parameters are reported.

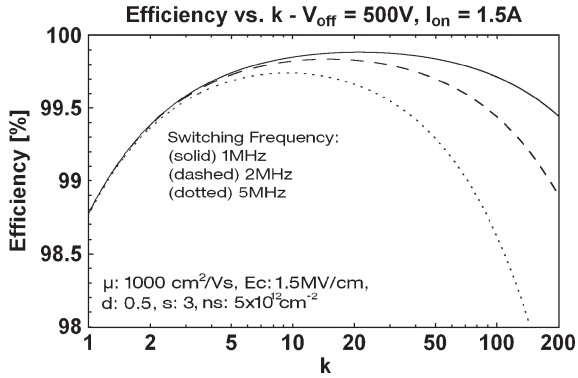

Fig. 8. Switching efficiency as function of k for three different switching frequencies of 1, 2, and 5 MHz. The most important simulated parameters are reported.

250 W/cm^2 as a safe power dissipation limit, the simulated value is more than three times higher than this limit; therefore, higher W_g and k should be chosen, with lower theoretical efficiency, as plotted in Fig. 5, in order to satisfy the power density constraint. As reported in Fig. 6, for a power dissipation density of 250 W/cm^2 and a charge density of 8×10^{12} cm^{-2}, the maximum theoretical efficiency that can be achieved is approximately 99.8%, which corresponds to the total losses of about 1.22 W.

The second case is for $V_{\rm off} = 800$ V and $I_{\rm on} = 1.5$ A, at a switching frequency of 1 MHz. The switching efficiency as a function of k for three different values of $n_s = 4 \times 10^{12}$, 8×10^{12}, and 1.5×10^{13} cm^{-2} is plotted in Fig. 7. In this case, the maximum theoretical efficiency, for a charge density of 1.5×10^{13} cm^{-2}, is for values of k of approximately 9. The corresponding L_{gd} and W_g are 16 μm and $\sim$0.8 cm, respectively. Being the active area of the device 1.28×10^{-3} cm^2, the resulting power dissipation density is higher than 1.3 kW/cm^2. Even in this case, based on the power density constraints, higher W_g and k have to be chosen, resulting in a lower theoretical switching efficiency.

The last case proposed points out the efficiency dependence on the switching frequency. For $V_{\rm off} = 500$ V and $I_{\rm on} = 1.5$ A, the efficiency as function of k is reported in Fig. 8 for three different switching frequencies of 1, 2, and 5 MHz. As shown, the optimum k as well as the maximum theoretical efficiency decreases as the switching frequency increases. This is in agreement with what is experimentally observed [7]. The increase in the power losses while increasing the switching frequency can be compensated, from the system-level point of view, by scaling the passive components of the switching system.

While the operating point coefficient s was kept constant in all three scenarios (see Figs. 5–8), this parameter does play an important role in both power losses minimization and safety operation of the device. From a safety operation point of view, low s means operating the device close to the breakdown condition, e.g., for $s = 1$, the OFF-state voltage is equal to the breakdown voltage. From the losses minimization point of view, lowering s translates into OFF-state losses increase but allows the design of shorter L_{gd}, thus, an overall reduction of the total losses. On the other hand, high s value allows a safer operation of the device but increase in the total losses.

IV. Conclusion

In conclusion, an analytical model predicting the power-switching behavior of a GaN-based HEMT has been developed. A complete analysis is presented in terms of the device's main physical parameters, i.e., 2-DEG carrier density, carrier mobility, active area geometry, and ON-state and OFF-state I–V operation points. The main conclusions of this paper can be summarized as follows.

1) In order to minimize the conduction losses, very high mobility and charge density have to be achieved in the 2-DEG. High values of k are desirable for the ON-state dc losses minimization.
2) The switching losses are directly proportional to the switching frequency. For a high-frequency operation, the switching losses increase has to be taken into account in the tradeoff while scaling the passive components of the switching system.
3) The maximum power dissipation density, thus, the minimum active area of the device, is limited by thermal dissipation capability. The choice of the ON-state and OFF-state I–V operating points plays an important role in the switching behavior of the device. A tradeoff between the active area of the device, the ON-state current, and the OFF-state voltage coefficients has to be found in order to maximize the overall efficiency. A process flow for a real device design has been proposed and discussed.

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