

Comparative study of self-aligned and nonself-aligned SiGe *p*-metal–oxide–semiconductor modulation-doped field effect transistors with nanometer gate lengths

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A self-aligned process used to fabricate *p*-type SiGe metal–oxide–semiconductor modulation-doped field effect transistors (MOS-MODFET) is described. Self- and nonself-aligned *p*-type Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3} MOS-MODFETs with gate-lengths from 1 μm down to 100 nm were fabricated. The dc and microwave characteristics of these devices are presented. In comparison with nonself-aligned devices, self-aligned devices exhibited higher extrinsic transconductances, lower threshold voltages, higher unity current gain cutoff frequencies f_T , and maximum oscillation frequencies f_{MAX} . Self-aligned MOS-MODFETs with a gate length of 100 nm exhibited an extrinsic transconductance of 320 mS/mm, an f_T of 64 GHz, and an f_{MAX} of 77 GHz. To our knowledge, these are the highest data ever reported for any MOS-type *p*-FETs with a SiGe channel. All these excellent performances were measured at very low drain and gate biases. © 2000 American Vacuum Society. [S0734-211X(00)11806-2]

I. INTRODUCTION

SiGe modulation-doped field effect transistors (MODFETs) have attracted much attention because of their excellent dc and rf performances.¹ However, these devices exhibited fairly high gate leakage currents, and hence small gate operation swings, limited by the Schottky barrier heights. SiGe metal–oxide–semiconductor MODFETs (MOS-MODFETs) with a gate dielectric layer between gate and channel exhibited extremely low gate leakage current.² But the devices exhibited high pinch-off voltages and threshold voltages as the gate length decreased down to 100 nm.³ A self-aligned process, which effectively reduces the parasitic resistances, can improve device performances dramatically. Adesida *et al.* reported a self-aligned 0.1 μm SiGe *p*-MODFET with extrinsic transconductance of 257 mS/mm, unity current gain cutoff frequency $f_T = 70$ GHz, and maximum oscillation frequency $f_{MAX} = 55$ GHz.^{4,5} Recently, Koester *et al.* reported a self-aligned 0.1 μm *p*-MODFET with a pure Ge channel that exhibited an extrinsic transconductance of 488 mS/mm.⁶ However, the relative high gate leakage current hinders the usefulness of these devices. In

this article, we report on the fabrication and characterization of self-aligned and nonself-aligned SiGe *p*-MOS-MODFETs with gate lengths down to 100 nm.

II. DEVICE LAYER STRUCTURE

The Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3} heterostructure was grown on a Si substrate by ultrahigh-vacuum chemical vapor deposition (UHV-CVD). The layer structure is shown in Fig. 1. The layer sequence started with a linearly step-graded Si_(1-x)Ge_x buffer layer relaxed to the lattice constant of Si_{0.7}Ge_{0.3}. A 1-μm-thick Si_{0.7}Ge_{0.3} buffer layer was followed by the modulation-doped structure which consisted of a 4 nm B-doped Si_{0.7}Ge_{0.3} supply layer at a doping density of 2×10^{18} cm⁻³, a 3 nm undoped Si_{0.7}Ge_{0.3} spacer, and a 4.5-nm-thick Si_(1-x)Ge_x channel graded from 0.8 to 0.7, and a 10 nm Si_{0.7}Ge_{0.3} cap layer. The layer exhibited a two-dimensional hole-gas mobility of 930 cm²/V s and a hole sheet density of 2.6×10^{12} cm⁻² as determined by Hall measurements at room temperature.

III. DEVICE FABRICATION

After the material growth, a silicon nitride gate dielectric layer was deposited by the jet-vapor-deposition (JVD)

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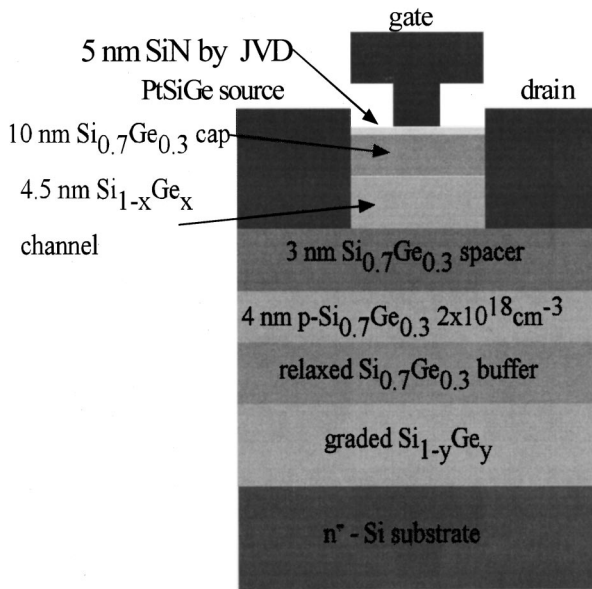
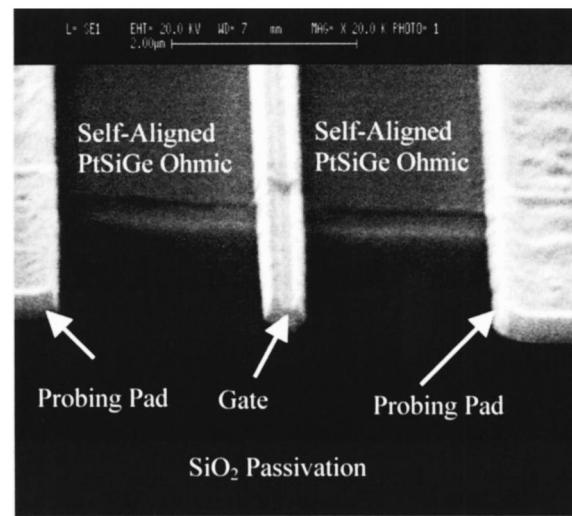
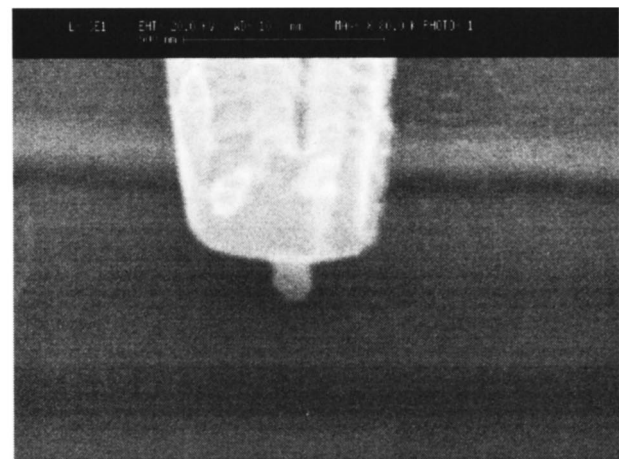


FIG. 1. Cross-sectional schematic of the UHV-CVD-grown *p*-type SiGe MOS-MODFET heterostructure.

method.⁷ To densify the film, postdeposition rapid thermal annealing was performed at 500 °C for 30 s. The physical thickness of the gate dielectric layer is 5 nm, equivalent to an oxide thickness of 3 nm. The FET active area was defined by optical lithography, followed by mesa etching in a CF₄ plasma. The etched surface was passivated by electron-beam-evaporated SiO₂ with a thickness equal to the mesa height. In the optical lithography, a chlorobenzene dip was used to facilitate the liftoff of the evaporated oxide. The liftoff of the evaporated oxide resulted in a planar surface for gate lithography and provided an insulating floor for microwave probing pads of devices. To fabricate self-aligned devices, T-shaped gates with various gate lengths from 1 μm down to 100 nm were defined by electron beam lithography using a trilayer resist system consisting of poly (methylmethacrylate) (PMMA) 950 K/PMMA-MAA/PMMA 50 K. The electron beam lithography was performed on a Cambridge EBMF-10.5 system at 40 kV accelerating voltage, 500 pA beam current, and 55 nm beam spot size. After exposure, the sample was developed in an MIBK:IPA=1:3 solution for 2 min at 21 °C. Then, Ti/Mo/Pt/Au metallization was evaporated and lifted off. The JVD SiN was etched by reactive ion etching (RIE) and 30 nm Pt ohmic metallization was evaporated by using the overhang of the T-shaped gates as shadow masks during RIE etching and evaporation. The sample was annealed at 350 °C for 5 min. The contact resistance is about 0.3 Ω mm. The Mo metal in the gates was used as a diffusion barrier during ohmic annealing. At last, Ti/Pt/Au pads were fabricated for dc and microwave probing. For comparison, nonself-aligned MOS-MODFETs were fabricated on another sample with the same layer structure. After mesa etching, SiO₂ passivation and planarization, and Pt metallization for ohmic contacts, Ti/Pt/Au T-shaped gates with variable gate length from 1 μm to 100 nm and probing pads were fabricated. The source–drain spacing of nonself-



(a)



(b)

FIG. 2. (a) SEM micrograph of a self-aligned *p*-type SiGe MOS-MODFET. (b) SEM micrograph of a T-shaped gate with a gate length of less than 100 nm and a head width of 0.5 μm.

aligned devices was 2 μm, except for devices with a gate length of 1 μm in which the source–drain spacing was 3 μm. The gate width was 100 μm for all devices. A scanning electron microscope (SEM) micrograph of a self-aligned MOS-MODFET is shown in Fig. 2(a). Figure 2(b) shows the micrograph of a T-shaped 100 nm gate with a 0.5-μm-wide head.

IV. DEVICE PERFORMANCE AND DISCUSSION

A. dc performance

The fabricated self-aligned and nonself-aligned *p*-type MOS-MODFETs were characterized at dc and microwave frequencies. The dc characteristics were measured using an HP4142B semiconductor parameter analyzer. Figure 3(a) shows the $I_{ds}-V_{ds}$ characteristics of a self-aligned and a nonself-aligned MOS-MODFET with a gate length of 100 nm. The maximum drain current I_{max} for the self-aligned device is 194 mA/mm and the I_{max} of the nonself-aligned

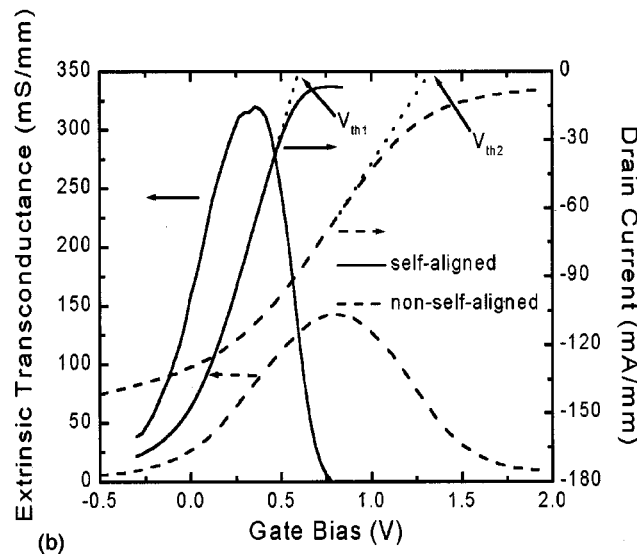
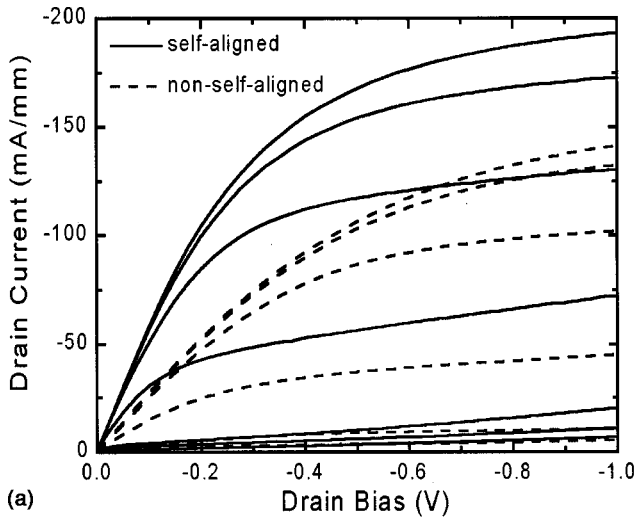


FIG. 3. (a) Current–voltage characteristics of a self-aligned MOS-MODFET and a nonself-aligned MOS-MODFET with a gate length of 100 nm. The gate bias was swept from -0.3 to 0.9 V in a step of 0.2 V for the self-aligned device and from -0.5 to 2.0 V in a step of 0.5 V for the nonself-aligned device. (b) Comparison of dc transfer characteristics of a self-aligned MOS-MODFET and a nonself-aligned MOS-MODFET with a gate length of 100 nm. The drain bias was -0.5 V for the self-aligned device and -1.0 V for the nonself-aligned device.

device is 142 mA/mm. The self-aligned devices exhibited greatly improved dc and rf performances in comparison to nonself-aligned devices while still maintaining extremely low gate leakage currents. Self-aligned devices exhibited lower knee voltages, lower pinch-off voltages, and lower threshold voltages. This is mainly attributed to the lower source series resistance of self-aligned devices. From our Hall measurement results, the sheet resistance $R_{sh} = \mu n q = 2.58 \times 10^3 \Omega/\text{square}$, where μ is the mobility, q is the electron charge, and n is the sheet carrier density. For nonself-aligned devices, the source access resistance $R_{ac} = R_{sh} \cdot L_{gs} = 2.45 \Omega \text{ mm}$, assuming that the gate is centrally located between the source and the drain. This is much higher than the ohmic contact resistance R_c . Therefore the source series resistance $R_s = R_{ac} + R_c = 2.75 \Omega \text{ mm}$. In contrast, the R_s for

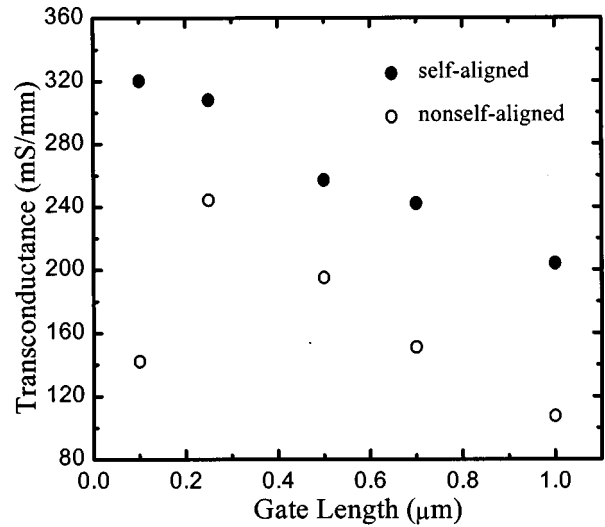


FIG. 4. Extrinsic transconductances of self-aligned and nonself-aligned SiGe p -MOS-MODFETs with various gate lengths.

self-aligned devices is only $0.81 \Omega \text{ mm}$, assuming that the overhang of the T gates is $0.2 \mu\text{m}$. The much lower source access resistance greatly enhances the drain current drive capability and the modulation efficiency. A comparison of the transfer characteristics of the foregoing self-aligned and nonself-aligned devices is shown in Fig. 3(b). The drain bias was -0.5 V for the self-aligned device and -1.0 V for the nonself-aligned device. The peak extrinsic transconductance g_m of 320 mS/mm for the self-aligned device was measured at $V_{gs} = 0.27$ V. This is the highest data ever reported for any p -type SiGe FETs with the same gate length and a SiGe channel. The g_m for the nonself-aligned device was 142 mS/mm at $V_{gs} = 0.82$ V. By defining the threshold voltage V_{th} as the gate bias intercept of the extrapolation of I_{ds} at the point of peak g_m , the threshold voltages of the self-aligned and nonself-aligned MOS-MODFET, V_{th1} and V_{th2} shown in Fig. 3(b), are 0.62 and 1.33 V, respectively. Figure 4 shows a comparison of extrinsic transconductances of self-aligned and nonself-aligned MOS-MODFETs with different gate lengths. Clearly, self-aligned devices exhibited higher extrinsic transconductances. For self-aligned devices, the extrinsic transconductance increases from 204 mS/mm for $1 \mu\text{m}$ devices to 320 mS/mm for 100 nm devices. For nonself-aligned devices, the extrinsic transconductance increases from 108 mS/mm for $1 \mu\text{m}$ devices to 245 mS/mm for $0.25 \mu\text{m}$ devices. However, 100 nm nonself-aligned devices exhibited an extrinsic transconductance of 142 mS/mm, which is lower than that of $0.25 \mu\text{m}$ devices. This is attributed to the short channel effect and the higher source access resistance because of the larger gate-to-source distance. As we calculated before, the R_{ac} of $0.25 \mu\text{m}$ and $0.1 \mu\text{m}$ nonself-aligned devices are 2.25 and $2.45 \Omega \text{ mm}$, respectively. Figure 5 shows threshold voltages of self-aligned and nonself-aligned MOS-MODFETs. Due to lower source access resistances, self-aligned devices exhibited clearly lower threshold voltages. As a result, nonself-aligned devices exhibited large gate

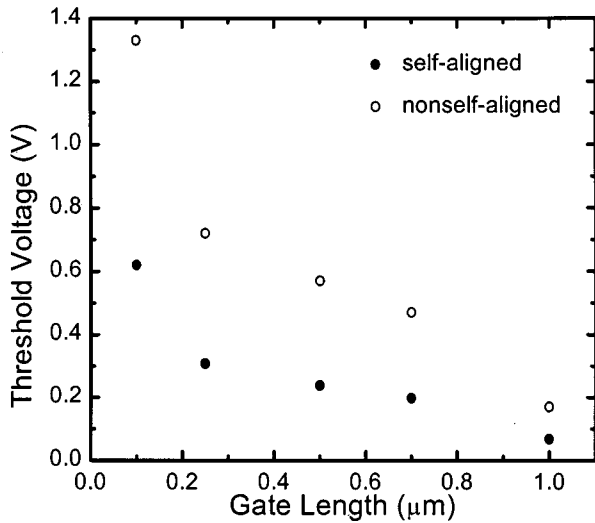


FIG. 5. Threshold voltages of self-aligned and nonself-aligned SiGe *p*-MOS-MODFETs with various gate lengths.

logic swing and better linearity. However, this advantage is a result of sacrificing higher extrinsic transconductance and microwave performance. The threshold voltages increase from 0.07 to 0.62 V for self-aligned devices and increase from 0.17 to 1.33 V for nonself-aligned devices. This indicates that nonself-aligned devices exhibit more severe short-channel effects and the self-aligned process can control the short-channel effects effectively.

B. rf performance

For rf characteristics, on-wafer measurements of *S* parameters from 1 to 35 GHz using a Cascade microtech probe and an HP8510B network analyzer have been used to determine unity current gain cutoff frequencies f_T and maximum oscillation frequencies f_{MAX} of the devices. The measured current gain $|h_{21}|$, maximum stable gain (MSG), and maximum available gain (MAG) versus frequency of a typical 100 nm nonself-aligned MOS-MODFET and a self-aligned MOS-MODFET are plotted against frequency in Fig. 6. The nonself-aligned device was biased at $V_{ds} = -0.9$ V and $V_{gs} = 0.8$ V and the self-aligned device was biased at $V_{ds} = -0.5$ V and $V_{gs} = 0.3$ V. The f_T and f_{MAX} were obtained by extrapolation of the current gain $|h_{21}|$ and maximum available gain using a -20 dB/decade slope. For the self-aligned device, an f_T of 64 GHz and an f_{MAX} of 68 GHz were obtained. At $V_{ds} = -1.0$ V and $V_{gs} = 0.3$ V, the device exhibited an f_T of 59 GHz and an f_{MAX} values of 77 GHz. To the authors' knowledge, these values are the highest data for any SiGe heterojunction MOSFETs. Moreover, these excellent dc and rf performances were measured at very low drain and gate biases. At $V_{ds} = -0.9$ V and $V_{gs} = 0.8$ V, the nonself-aligned one exhibited an f_T of 38 GHz and an f_{MAX} value of 55 GHz. Figure 7 shows the f_T and f_{MAX} of self-aligned and nonself-aligned MOS-MODFETs as a function of gate length. The $f_T(f_{MAX})$ values of self-aligned devices are 40 (49), 16 (28), 9 (19), and 5 (10) GHz for 0.25, 0.5, 0.7, and 1.0 μ m devices, respectively. The f_T and f_{MAX} val-

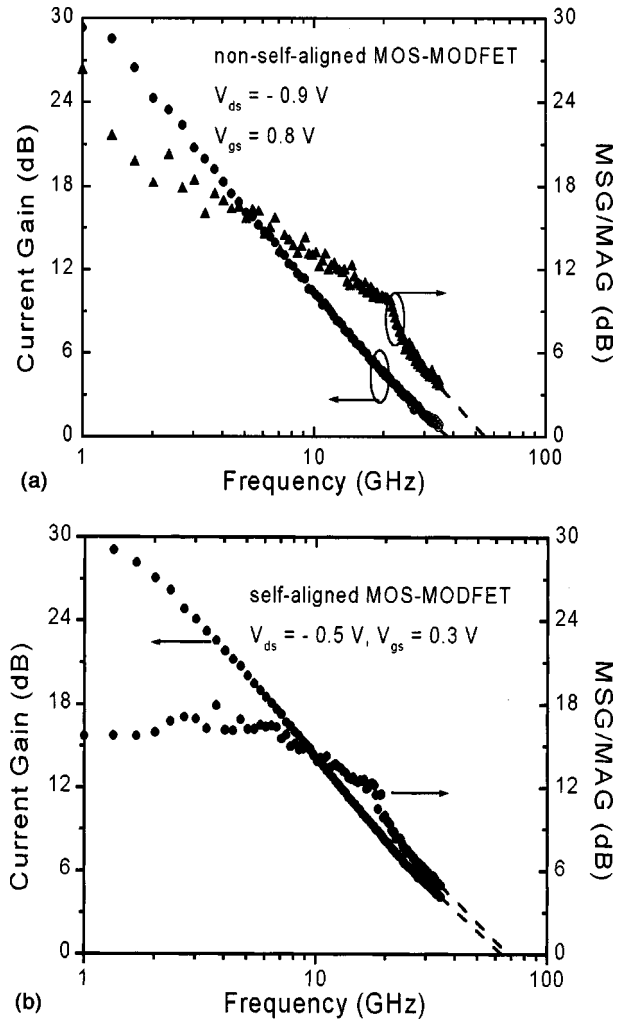


FIG. 6. Measured current gain $|h_{21}|$, MSG, and MAG vs frequency for a typical 100 nm nonself-aligned MOS-MODFET (a) and a 100 nm self-aligned MOS-MODFET (b) with 100 μ m gate width. The nonself-aligned device was biased at $V_{ds} = -0.9$ V and $V_{gs} = 0.8$ V and the self-aligned device was biased at $V_{ds} = -0.5$ V and $V_{gs} = 0.3$ V.

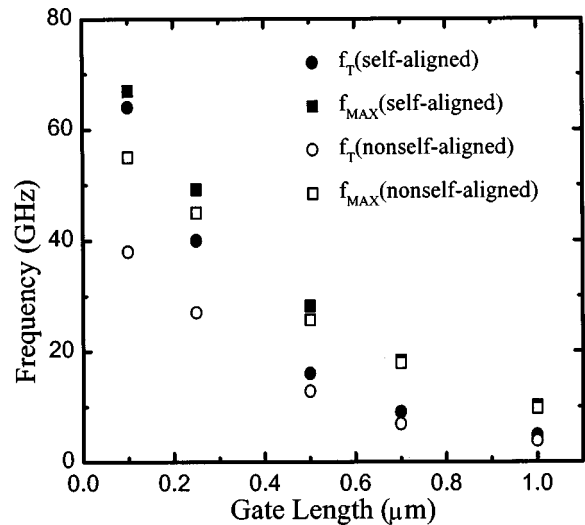


FIG. 7. Unity current gain cutoff frequencies f_T and maximum oscillation frequencies f_{MAX} of self-aligned and nonself-aligned SiGe *p*-MOS-MODFETs with various gate lengths.

ues for nonself-aligned devices are 27 (45), 13 (26), 7 (18), and 4 (10) for 0.25, 0.5, 0.7, and 1.0 μm devices, respectively.

V. CONCLUSION

In summary, we have developed a self-aligned process to fabricate SiGe p -type MOS-MODFETs. Self- and nonself-aligned p -type SiGe MOS-MODFETs with variable gate length from 1 μm to 100 nm were fabricated. The dc and microwave performances of the devices were characterized. For a given gate length, the self-aligned devices exhibited higher extrinsic transconductance, lower threshold voltages, higher maximum drain current, f_T , and f_{MAX} . The 100 nm self-aligned devices exhibited an extrinsic transconductance of 320 mS/mm. To our knowledge, this is the highest data ever reported for any p -FETs with a SiGe channel. An f_T of 64 GHz and an f_{MAX} of 77 GHz were measured. These values are the highest data for any MOS-type SiGe p -FETs. In comparison with self-aligned devices, nonself-aligned devices exhibited larger gate logic swing because of lower transconductances. dc results show that the self-aligned process controls short-channel effects effectively.

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