PERGAMON

Solid-State Electronics 46 (2002) 743–746

SOLID-STATE ELECTRONICS

DC and microwave performance of recessed-gate GaN MESFETs using ICP-RIE

C. Lee [a], W. Lu [a,*], E. Piner [b], I. Adesida [a]

[a] *Microelectronics Laboratory and Department of Electrical and Computer Engineering, University of Illinois at Urbana—Champaign, Urbana, IL 61801, USA*

[b] *Epitronics/ATMI, Phoenix, AZ 85027, USA*

Received 15 July 2001; accepted 22 August 2001

Abstract

The fabrication and characterization of GaN MESFETs grown on sapphire recessed using inductively-coupled-plasma reactive ion etching (ICP-RIE) are reported for the first time. The MESFETs were recessed using a Cl_2/Ar plasma in ICP-RIE, and the drain current was monitored during recess. The devices with a gate length of 0.25 μm exhibited a peak extrinsic transconductance of 36 mS/mm and a threshold voltage of −3.7 V. The unity current gain cutoff frequency f_T and maximum frequency of oscillation f_{max} were measured to be 28 and 55 GHz, respectively at room temperature. This recessed-gate process produced high extrinsic transconductances and lower threshold voltages compared with those of unrecessed GaN MESFETs. Also, the values of f_T and f_{max} are at least twice the highest frequency data ever reported for GaN MESFETs. The influence of substrate temperature on the DC and microwave characteristics is also reported.

Keywords: GaN; MESFET; Inductively-coupled-plasma reactive ion etching; Gate recess

1. Introduction

With recent intense research efforts, GaN-based field effect transistors (FETs) have emerged as a promising candidate for high power and high temperature microwave applications. These devices' impressive performance is due to the material's properties, such as wide band gap, high breakdown field, and high electron saturation velocity. To date, most of the research efforts have been on AlGaN/GaN heterostructure FETs (HFETs). However, a few published reports on GaN MESFETs, both simulated and experimental, demonstrated that these devices have potential for power applications in the low microwave frequency range [1–8]. Recently, Gaquiere et al. reported encouraging power performance on a GaN MESFET, which exhibited a power density of 2.2 W/mm with a power added efficiency of 27% at $V_{DS} = 30$ V and $V_{GS} = -2$ V at 2 GHz [3]. From published results, GaN MESFETs have exhibited extrinsic transconductance G_m and unity current gain cutoff frequency f_T in the range of 23–33 mS/mm and 5–11 GHz, respectively [3–6]. These reports have so far mostly dealt with unrecessed MESFETs. The high pinch-off voltages hinder the usefulness of these unrecessed MESFETs. An alternative recessed-gate structure is extensively used in fabricating HFETs or MESFETs in other III–V material systems. This structure, which utilizes a highly doped cap layer on top of the channel layer, leads to improved ohmic contact resistance, lower pinch-off voltages, and higher modulation efficiencies due to shorter gate-to-channel distances. Gate recessing involves etching away the highly doped cap layer with the gate metal deposited in the recessed area. Initial efforts on gate recessing for GaN FETs have been

* Corresponding author. Tel.: +1-217-333-4182; fax: +1-217-244-6375.

E-mail address: wulu@capone.micro.uiuc.edu (W. Lu).

0038-1101/02/$ - see front matter
PII: S0038-1101(01)00292-1

demonstrated using photoelectrochemical wet etching [7,8], reactive ion etching (RIE) [5], and electron-cyclotron-resonance RIE [9]. The recessed-gate MESFETs produced G_ms and f_Ts in the range of 33–41 mS/mm and 5–12 GHz, respectively, in which the wet-recessed devices demonstrated the highest previously reported f_T of 12 GHz [5,7–9]. To minimize the ion-induced damage in a plasma etch process, the RIE system's substrate bias must be low. Inductively-coupled-plasma (ICP) RIE allows separate control of the ion energy and plasma density, which leads to high GaN etch rates while maintaining a low substrate bias [10]. Therefore, ICP-RIE is ideal for obtaining low-damage recess etching. In this letter, for the first time, we report the process and the DC and RF performances of recessed-gate GaN MESFETs fabricated using a PlasmaTherm Shuttlelock 700 ICP-RIE system. This ICP-RIE recessed-gate process has enabled GaN MESFETs to achieve excellent RF performances compared with those previously reported. This process should be applicable to the fabrication of recessed-gate AlGaN/GaN high electron mobility transistors for high frequency applications.

2. Device fabrication

The device structure consisted of a 2 μm semi-insulating GaN buffer, a 2000 Å lightly doped ($\sim 2 \times 10^{17}$ cm^{-3}) active channel, and a 400 Å heavily doped ($>5 \times 10^{18}$ cm^{-3}) GaN cap layer grown on sapphire substrate by metal-organic chemical vapor deposition. Mesa isolation, which defined a total device width of 100 μm, was formed using an ICP-RIE in a Cl_2/Ar plasma. The source and drain ohmic contacts were formed by rapid-thermally annealing in a Ti/Al/Ti/Au metallization scheme at 800 °C for 30 s, which yielded typical contact resistance R_c of $\sim 0.15\ \Omega$ mm and sheet resistance R_{sheet} of 611 Ω/sq. To perform the gate recess, PECVD-deposited Si_3N_4 was used as an etching mask. One-micron recess windows, centered between the source and drain, were patterned in the Si_3N_4 mask. The recess etch was performed using a Cl_2/Ar plasma with a gas flow rate of 15/5 sccm, a pressure of 5 mT, an induced bias of −50 V, and an ICP coil power of 300 W. The etch rate under these conditions was typically ∼200 Å/min. The effect of the recess etch was carefully monitored by measuring the decrease of the drain current as a function of etching time as shown in Fig. 1. The drain current, which was 98 mA at $V_{DS} = 10$ V after 30 s of etching, decreased significantly at the beginning and decreased very slowly when the cap layer was completely removed. After recess, the Si_3N_4 was removed using a wet etchant. The sample was then rapid-thermally annealed at 700 °C in N_2 ambient for 1 min to minimize any etch-induced damage and restore the Schottky barrier height of the etched surface to that of an unetched surface [11].

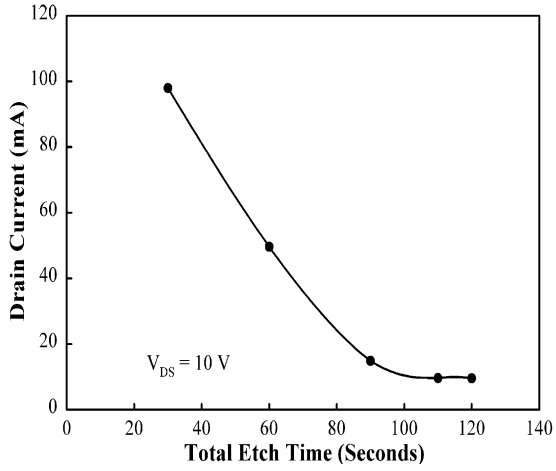

Fig. 1. Drain current as a function of gate-recess etch time where $V_{DS} = 10$ V.

Finally, a mushroom-shaped 0.25 μm Ni/Au Schottky gate was fabricated by electron beam lithography. The source–drain spacing was 3 μm.

3. Results and discussion

Fig. 2 shows the I_{DS}–V_{DS} characteristics of a typical device at room temperature. The gate was biased from 0 to −6 V with a step of −1 V. An I_{DSS} of 137 mA/mm was measured at $V_{DS} = 15$ V. The device exhibited excellent channel pinch-off characteristics. The device was completely pinched off at a gate bias of −5 V, which is much

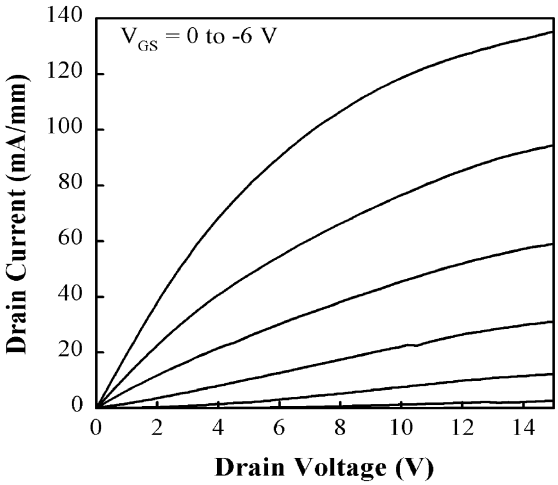

Fig. 2. I_{DS}–V_{DS} characteristics of a typical 0.25 μm device at room temperature.

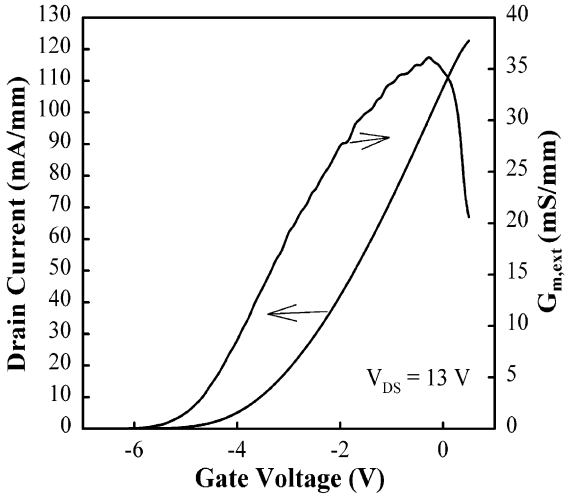

Fig. 3. DC transfer characteristics of a typical 0.25 μm devices at room temperature.

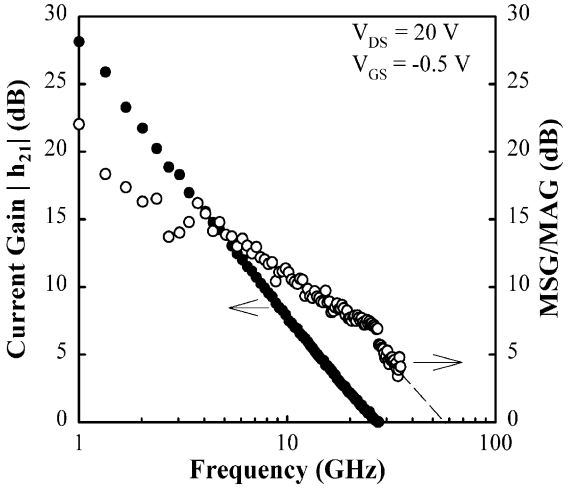

Fig. 4. Short-circuit gain and maximum stable and available gain (MSG/MAG) as a function of frequency.

lower than that of unrecessed MESFETs, as high as −13 V [4]. However, as shown in Fig. 2, the device exhibited extremely high knee voltage of approximately 8–9 V, which might be caused by a high density of traps within the channel material. The measured G_{mext} and I_{DS} as a function of gate bias are shown in Fig. 3. The peak G_{mext} was 36 mS/mm at a V_{GS} of −0.27 V, which is comparable to the peak G_{mext} previously reported [3–9]. The source access resistance $R_{acc} = R_{sheet}L_{GS} = 0.84\ \Omega$ mm for a gate length of 0.25 μm and a source–drain spacing of 3 μm. The intrinsic transconductance of the device is calculated to be 37.33 mS/mm. The threshold voltage is defined as the gate voltage intercept of the linear extrapolation of the I_{DS} versus V_{GS} characteristics at the maximum transconductance point. Using this technique, the threshold voltage was −3.7 V. The gate–source Schottky diode characteristics for a gate width of 50 μm was measured, and the diode current was as low as −0.38 mA/mm at a bias of −45 V.

The small signal RF performance was measured using an HP 8510B network analyzer from 1 to 35 GHz. At a drain bias of 20 V and a gate bias of −0.5 V, the f_T and f_{max} were measured to be 28 and 55 GHz, respectively, as shown in Fig. 4. To the best of the authors' knowledge, these results are at least twice the highest frequency data ever reported for GaN MESFETs. The excellent RF performance is attributed to better modulation of the channel. The DC and RF results show that this process was effective in removing the cap layer and limiting the etch-induced damage.

The device performance was further examined as a function of temperature. The drain current and transconductance were measured from −55 to 200 °C at a fixed gate bias of −0.5 V and a drain bias of 15 V. Fig. 5

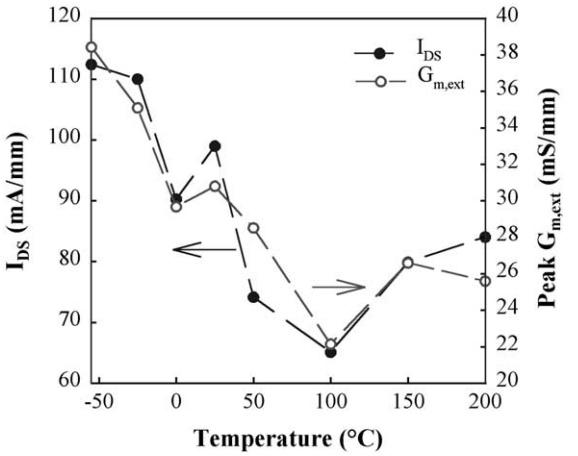

Fig. 5. The drain current and peak transconductance as a function of temperature ranging from −55 to 200 °C at V_{DS} = 15 V and V_{GS} = −0.5 V.

shows that both I_{DS} and G_{mext} decreased as the temperature was increased from −55 to 100 °C as the mobility degrades as a function of temperature. When the temperature was further increased to 200 °C, the drain current and transconductance began to rise. This phenomenon might be caused by the emission of charges from the traps into the channel at high temperature [12]. The addition of free charges increases the conductance of the channel and causes the observed DC trend at high temperature. The temperature dependence of the microwave performance was investigated by measuring the f_T and f_{max} from −55 to 200 °C while keeping the drain and gate bias at 20 and −0.5 V, respectively. Fig. 6

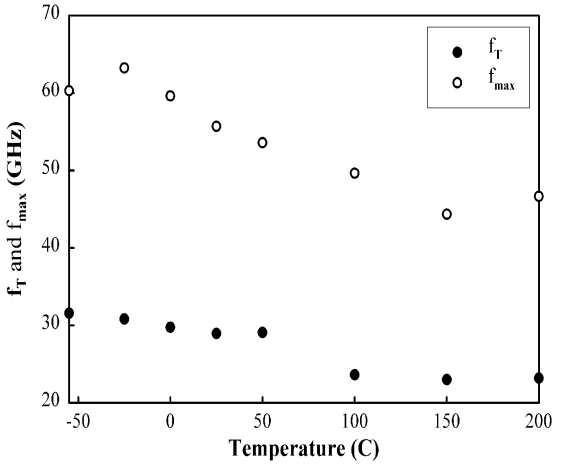

Fig. 6. The measured f_T and f_{max} as a function of temperature ranging from −55 to 200 °C at $V_{DS} = 20$ V and $V_{GS} = -0.5$ V.

shows that the values of f_T do not degrade significantly as a function of temperature. A 30% change was observed as f_T and f_{max} decreased from 32 and 60 GHz at −55 °C to 23 and 46 GHz at 200 °C, respectively. Current efforts are being directed to device modeling in order to fully understand this temperature dependence.

4. Conclusion

We have developed a low-damage, gate-recess procedure for GaN-based FETs using an ICP-RIE system. The GaN MESFETs with recessed-gates demonstrated excellent DC and microwave performance. The devices exhibited a high peak transconductance of 36 mS/mm and a much lower threshold voltage of −3.7 V in comparison with unrecessed MESFETs. Record high f_T and f_{max} of 28 and 55 GHz were achieved, respectively. The DC and RF performance of these devices as a function of temperature were also characterized. At high temperature, a decrease in channel resistance and a rise in drain current were observed. The microwave performance degraded slightly as the temperature was increased from −55 to 200 °C. With further optimization of the recess process, better high frequency performances for recessed-gate GaN MESFETs and HFETs are expected.

Acknowledgements

This work was supported by US Air Force under contract AF# 98-46029 and by ONR under contract N00014-01-1-1000 monitored by Dr. J. Zolper.

References

[1] Farahmand M, Brennan KF. Full band Monte Carlo simulation of zincblende GaN MESFET's including realistic impact ionization rates. IEEE Trans Electron Dev 1999;46:1319–25.
[2] Shin MW, Trew RJ. GaN MESFETs for high-power and high-temperature microwave applications. Electron Lett 1995;31:498–500.
[3] Gaquiere C, Trassaert S, Boudart B, Crosnier Y. High-power GaN MESET on sapphire substrate. IEEE Microwave Guided Wave Lett 2000;10:19–20.
[4] Egawa T, Nakamura K, Ishikawa H, Jimbo T, Umeno M. Characteristics of a GaN metal semiconductor field-effect transistor grown on a sapphire substrate by metalorganic chemical vapor deposition. Jpn J Appl Phys Part 1 1999;38:2630–3.
[5] Binari SC, Doverspike K, Kelner G, Dietrich HB, Wickenden AE. GaN FETs for microwave and high-temperature applications. Solid-State Electron 1997;41:177–80.
[6] Yoshida S, Suzuki J. High-temperature reliability of GaN metal semiconductor field-effect transistor and bipolar junction transistor. J Appl Phys 1999;85:7931–4.
[7] Ping AT, Selvanathan D, Youtsey C, Piner E, Redwing J, Adesida I. Gate recessing of GaN MESFETs using photoelectrochemical wet etching. Electron Lett 1999;35:2140–1.
[8] Lee WS, Choi YH, Chung KW, Moon DC, Shin MW. High temperature performance of recessed gate GaN MESFETs fabricated using photoelectrochemical etching process. Electron Lett 2000;36:265–7.
[9] Ren R, Lothian JR, Chen YK. Recessed gate GaN field effect transistor. Solid-State Electron 1997;41:1819–20.
[10] Pearton SJ, Zolper JC, Shul RJ, Ren R. GaN: processing, defects, and devices. J Appl Phys 1999;86:28.
[11] Ping AT, Schmitz AC, Adesida I, Asif Khan M, Chen Q, Yang J. Characterization of reactive ion etching-induced damage to n-GaN surface using Schottky diodes. J Electron Mater 1997;26(3):266–71.
[12] Trassaert S, Boudart B, Gaquiere C, Theron D, Crosniere Y, Huet F, Poisson MA. Trap effects studies in GaN MESFETs by pulsed measurements. Electron Lett 1999;35:1386–8.