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FABRICATION OF SELF-ALIGNED T-GATE AlGaN/GaN HIGH ELECTRON MOBILITY TRANSISTORS

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Self-aligned AlGaN/GaN high electron mobility transistors (HEMTs) are fabricated and the direct current and radio frequency small signal performance of self-aligned devices is characterized in comparison with non-self-aligned devices. An ultra-thin Ti/Al/Ti/Au ohmic metal scheme is used for gate to source and drain self-alignment. To suppress the gate leakage current, the ohmic contact annealing of self-aligned devices is performed in a furnace. The self-aligned devices with 0.25 μm gate-length and 100 μm gate-width exhibit good pinch-off characteristics. The maximum drain current at a gate bias of 1 V is 620 mA/mm for self-aligned HEMTs, and 400 mA/mm for non-self-aligned devices, respectively. A maximum extrinsic transconductance of 146 mS/mm is measured in self-aligned devices, while non-self-aligned HEMTs show only a peak g_m of 92 mS/mm. The self-aligned devices exhibit an extrinsic f_T of 39 GHz and an f_{MAX} of 130 GHz, whereas non-self-aligned HEMTs show an f_T of 15 GHz and an f_{MAX} of 35 GHz.

1 Introduction

AlGaN/GaN HEMTs have excellent potential for high frequency, high power, and high temperature applications because of their unique material properties such as high electron peak velocity, high breakdown voltage, high electron density, and high thermal and chemical stability. Significant progress in device performance has been demonstrated in the last few years.[1-8] However, further improvements of AlGaN/GaN HEMTs rely on the improvement of material quality and further reduction of parasitic resistance. To minimize the source access resistance, Ching-Hui Chen et al. re-grew an n+ GaN layer self-aligned to the gate to reduce the source and drain ohmic contacts using a re-grown process.[9] Another effective way is to reduce the distances between the gate to source and drain as closely as possible, which has been proved to be an effective methodology to improve device speed performance by Si, III-V devices. Self-aligned AlGaN/GaN HEMTs are very attractive because of the minimized source access resistance due to the reduction of separation from gate to source and drain. In the self-aligned process, the thin ohmic level follows the gate metallization. It is crucial that the ohmic annealing temperature should not exceed some critical point above which the Schottky gate characteristics are significantly degraded. However, the thick metal scheme and high processing temperature of ohmic contacts on III-nitrides hinder the realization of self-aligned devices. So far, little has been reported on self-aligned AlGaN/GaN HEMTs. Recently, it was demonstrated that the breakdown voltage of AlGaN/GaN HEMTs with Ni/Au gate could be significantly improved after a thermal annealing process even at 750

°C in a furnace,[10, 11] which makes the fabrication of self-aligned devices feasible. In this letter, we report self-aligned AlGaN/GaN HEMTs with thin ohmic contacts annealed at 750 °C and compare direct current (DC) and radio frequency (RF) small signal characteristics of self-aligned with those of non-self-aligned AlGaN/GaN HEMTs fabricated on the same material.

2 Fabrication

Fig. 1 shows the cross-sectional view of self-aligned T-gate AlGaN/GaN HEMT. The epilayer of AlGaN/GaN HEMT structure was grown by metal-organic chemical vapor deposition on (0001) sapphire substrate. The epilayer consists of 40 nm AlN nucleation layer, 3 μm of undoped GaN, and 20 nm undoped $Al_{0.3}Ga_{0.7}N$. The sheet resistance of epilayer is 432 Ω/sq. For device fabrication, device isolation was obtained with shallow mesa dry etching in a chlorine-based plasma. The drain-source first-level ohmic contacts with 3.5-μm spaces were deposited with Ti/Al/Pd/Au and annealed at 850 °C for 30 s in a rapid thermal annealing system. This level was included to reduce the contact resistance of the ohmic contacts. Electron-beam lithography and Ni/Au metallization were performed for gate contacts with a gate-length of 0.25 μm. The Ti/Al/Ti/Au thin ohmic layer with a total thickness of 80 nm was deposited and annealed. The thin ohmic layer is self-aligned to the T-gate using gate overhangs as a shadow mask. The annealing processing condition is chosen to make sure the formation of ohmic contact and the suppression of gate leakage current. Ni/Au layer was deposited for overlay. Fig. 2 is a SEM photograph of a typical 0.25 μm self-aligned AlGaN/GaN HEMT. It shows very smooth morphology of the thin ohmic layer even after annealing.

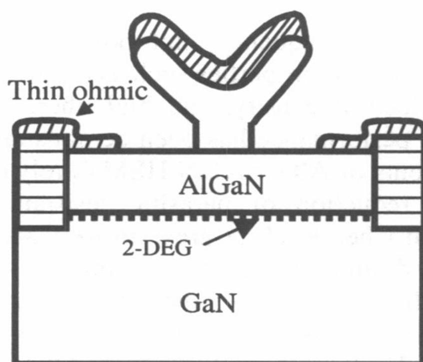

Fig. 1. Cross sectional view of self- aligned T-gate AlGaN/GaN HEMT.

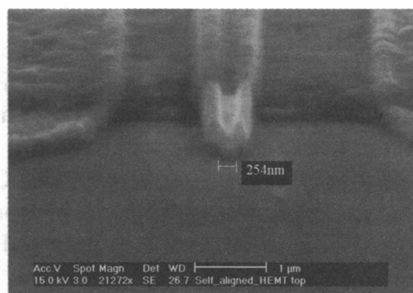

Fig. 2. SEM photograph of self-aligned T-gate AlGaN/GaN HEMT

3 Results and Discussion

In fabrication of self-aligned HEMTs, the formation of thin ohmic layer is crucial. Transmission line measurement (TLM) with Ti/Al/Ti/Au metal scheme was used to

optimize annealing condition. Fig. 3 shows the current-voltage (I-V) characteristics between two contact pads with a spacing of 4 μm after annealing. It exhibits a linear relationship between current and bias voltage, showing good ohmic characteristics. The pad-to-pad resistances calculated from I-V data for different pad spaces are given in Fig 4. The ohmic contact resistivity and contact resistance of the thin ohmic layer are determined to be 3.8×10^{-6} Ωcm^2 and 0.8 Ωmm, respectively.

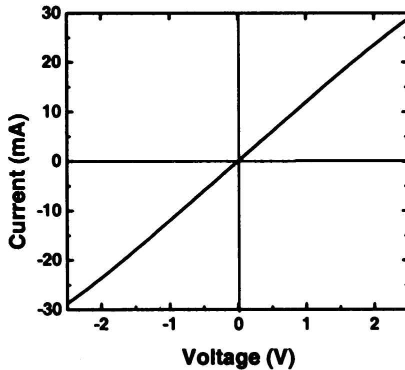

Fig. 3. Typical I-V characteristic between two ohmic contacts on AlGaN/GaN heterostructures with ultrathin Ti/Al/Ti/Au metallization.

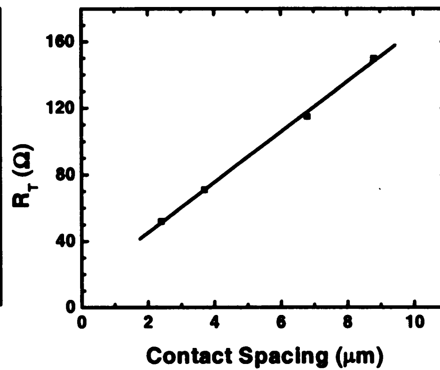

Fig. 4. Resistances of TLM pattern as a function of contact spacings.

Fig. 5 shows the typical drain current characteristics of self-aligned (solid lines) and non-self aligned AlGaN/GaN HEMTs with 0.25-μm gate-length and 100-μm gate-width. Despite the small separation between gate to source and drain, self-aligned devices exhibit excellent pinch-off behaviors. The gate biases range from –7 V to 1 V with a step of 1 V. The maximum drain current at a gate bias of 1 V and pinch-off voltage are 620 mA/mm and –7 V for self-aligned HEMTs, and 400 mA/mm and – 6 V for non-self-

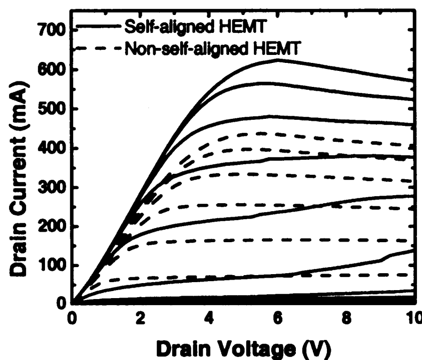

Fig. 5. I_D-V_D characteristics of self-aligned (solid lines) and non-self-aligned (dashed lines) AlGaN/GaN HEMTs. The gate voltage is in the range of -7 V to 1 V in a step of 1 V.

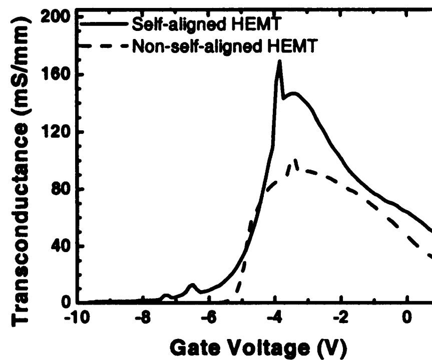

Fig. 6. Transconductance of self-aligned (solid line) and non-self-aligned (dashed line) AlGaN/GaN HEMTs. The drain bias is 8 V.

aligned devices, respectively. The knee voltages of both type devices are 4 V. At gate biases of 1, 0, and–1 V, the current-voltage characteristics of both type devices at drain bias voltage higher than 8 V exhibit negative differential resistance characteristic due to the poor thermal conductivity of sapphire substrates. Fig. 6 shows the typical transfer characteristics of self-aligned (solid lines) and non-self-aligned devices (dashed lines). As a result of reduced spacing between gate to source and drain, self-aligned devices exhibited a maximum extrinsic transconductance (g_m) of 146 mS/mm at a gate voltage of – 3.4 V and at a drain bias voltage of 6 V, while non-self-aligned HEMTs exhibited only a peak g_m of 92 mS/mm at a gate of – 3.1 V. The g_m improvement is attributed to the smaller source access resistance of self-aligned devices, $R_{acc} = R_{sh} \times L_{gs} = 1\ \Omega$, where R_{sh} is the sheet resistance and L_{gs} is the gate-to-source distance. For comparison, the non-self-aligned devices have a R_{acc} of 6.3 Ω. From the gate-bias intercept of the extrapolation of drain current curve, the threshold voltages of self-aligned and non-self-aligned devices are determined to be – 5.5 V and – 4.8 V, respectively. Fig. 7 shows gate-drain Schottky diode current characteristics of self-aligned devices. During measurements, the drain was shorted to the source. The gate-to-drain leakage current was determined to be 2 x 10^{-8} A at a gate bias of – 40 V, even though the gate to drain and source space is as small as only about 0.2 μm. This remarkably small gate leakage current is attributed to the reduction of trapping effects due to thermal annealing after formation of gate metallization.[12]

For microwave characteristics, on-wafer measurements of small signal S-parameters were performed from 1 to 50 GHz to determine f_T and f_{MAX}. Fig. 8 shows the plots of current gain $|h_{21}|$ and maximum stable power gain (MSG) and maximum available gain (MAG) versus frequency for self-aligned (solid lines) and non-self-aligned (dashed lines) devices. f_T and f_{MAX} were determined by the extrapolation of $|h_{21}|$ and MSG/MAG with –20 dB/decade slope. The self-aligned devices exhibit an extrinsic f_T of 39 GHz and an f_{MAX} of 130 GHz at a gate bias of – 3.5 V and a drain bias of 5 V, whereas non-self-aligned HEMTs show an f_T of 15 GHz and an f_{MAX} of 35 GHz at a gate bias of – 3 V and a drain bias of 6 V.

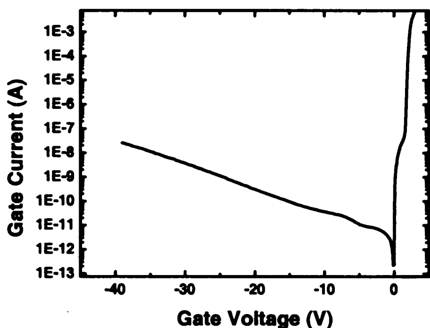

Fig. 7. Gate current characteristics of self-aligned AlGaN/GaN HEMTs as a function of gate bias.

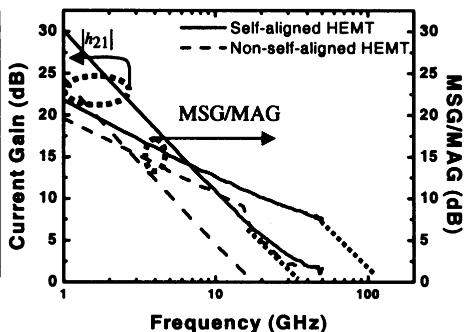

Fig. 8. Current gain and maximum stable/available power gain of 0.25 μm self-aligned and non-self-aligned AlGaN/GaN HEMTs.

4 Conclusions

We have fabricated self-aligned T-gate AlGaN/GaN HEMTs with 0.25 μm gate-length on a sapphire substrate. The self-aligned devices exhibit good pinch-off characteristics and very low gate leakage current. The maximum drain current at $V_g = 1$ V, g_m, f_T, and f_{MAX} of self-aligned devices are improved from 400 mA/mm to 620mA/mm, from 92 mS/mm to 146 mS/mm, from 15 GHz to 39 GHz, and 35 GHz to 130 GHz, respectively. All of these improvements are attributed to the smaller parasitics of self-aligned devices.

Acknowledgements

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