Frequency dispersion in III-V metal-oxide-semiconductor capacitors

Susanne Stemmer,[1,a)] Varistha Chobpattana,[1] and Siddharth Rajan[2]
[1]*Materials Department, University of California, Santa Barbara, California 93106-5050, USA*
[2]*Department of Electrical and Computer Engineering, The Ohio State University, Columbus, Ohio 43210, USA*

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A recombination-controlled tunneling model is used to explain the strong frequency dispersion seen in the accumulation capacitance and conductance of dielectric/*n*-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors. In this model, the parallel conductance is large when, at positive gate biases, the metal Fermi level lines up with a large density of interface states in the $In_{0.53}Ga_{0.47}As$ band gap. It is shown that the model explains in a semi-quantitative manner the experimentally observed capacitor characteristics, including a peak in parallel conductance/frequency (G_p/ω) versus log frequency curves at positive gate bias and the dependence of the frequency dispersion on the dielectric thickness. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4724330]

Extensive research activities have focused on developing dielectrics, such as Al_2O_3 and HfO_2, on *n*-$In_{0.53}Ga_{0.47}As$ for metal-oxide-semiconductor field effect transistors (MOSFETs).[1] Advantages of $In_{0.53}Ga_{0.47}As$ as a channel material include its low electron effective mass, high saturation velocity, low intervalley scattering and that it is lattice-matched to InP.[2] One of the most serious challenges for III-V channel MOSFETs is the inherently large density of traps (D_{it}) at the dielectric/III-V semiconductor interface. The interface trap state distribution in the band gap depends largely on the specific III-V semiconductor.[3–6] For example, the D_{it} of dielectric/*n*-$In_{0.53}Ga_{0.47}As$ interfaces is sufficiently low to achieve band bending (semiconductor Fermi level movement) in the upper half of the semiconductor band gap under an applied voltage,[7,8] resulting in significant device demonstrations.[9,10] One of the most important unresolved issues, however, remains the lack of understanding of the large frequency dispersion that is observed in accumulation, for example, for dielectrics on *n*-$In_{0.53}Ga_{0.47}As$. This dispersion is particularly severe for more highly scaled, high-capacitance-density metal-oxide-semiconductor capacitor (MOSCAP) structures, such as the one shown in Fig. 1, which has an equivalent oxide thickness (EOT) of about 1.2 nm.[11] Pronounced frequency dispersion is seen in the capacitance [Fig. 1(a)] as well as ac conductance [Fig. 1(b)] at positive gate biases.

Frequency dispersion arises when trap states communicate with the semiconductor conduction or valence bands.[12,13] The conductance is maximized when the semiconductor Fermi level is aligned with the trap states, and the ac signal causes a change in the trap occupancy. Curves of G_p/ω versus log frequency, where G_p is the equivalent parallel conductance and ω the radial frequency, show a maximum when $\omega\tau \approx 1$ (τ is the trap recombination time constant). By analyzing the parallel conductance, the trap state density, their position in the band gap, and other trap parameters can be extracted.[13,14] For example, the frequency dispersion ("hump") seen at negative gate biases in the capacitance-voltage characteristics [Fig. 1(a)] and around 0 V in the conductance-voltage curves [Fig. 1(b)] is due to midgap traps.[15,16] In accumulation (i.e., at sufficiently large positive gate bias for n-type channels), however, the semiconductor Fermi level moves deep into the conduction band, due to the low conduction band density of states (DOS) of

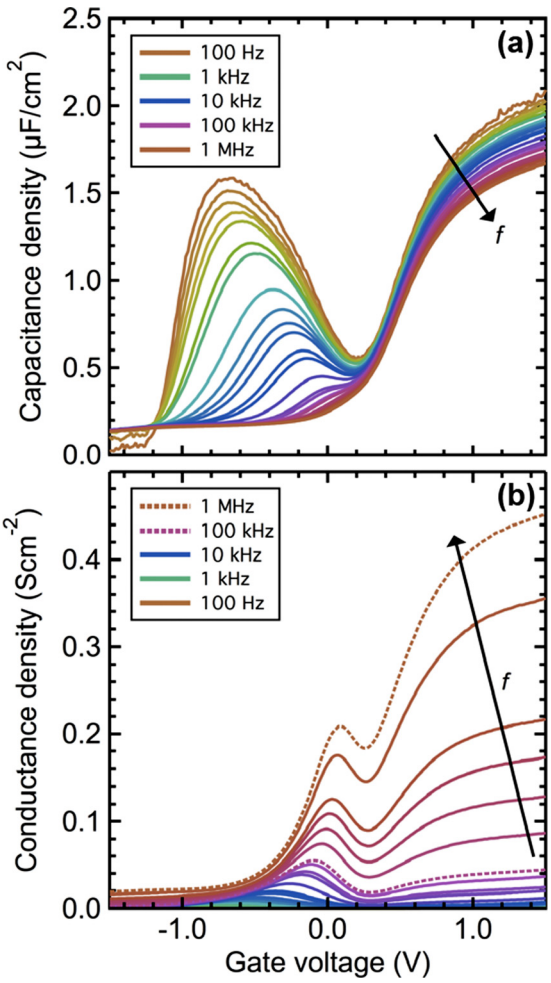

FIG. 1. (a) Capacitance-voltage and (b) conductance-voltage characteristics of a 3 nm thick $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP with a Ni electrode. The doping in the $In_{0.53}Ga_{0.47}As$ was Si (1×10^{17} cm^{-3}). The detailed fabrication procedure has been described elsewhere.[30] The conductance is the equivalent parallel conductance extracted from the measured device admittance.[15,31]

[a)]Author to whom correspondence should be addressed. Electronic mail: stemmer@mrl.ucsb.edu.

III-V semiconductors.[17–19] The recombination time constants of interface states that line up with the semiconductor Fermi level at positive gate bias are expected to be very short and are thus *not* expected to give rise to a strong frequency dispersion.[20]

A possible explanation put forward in the recent literature is that the frequency dispersion in accumulation is due to "border traps," which are defects that reside in the oxide.[20–23] Tunneling into these defects is associated with a time constant that depends on their distance to the interface, giving rise to frequency dispersion.[13,20] It is reasonable to expect that the type and spatial distribution of border traps, and thus the frequency dispersion characteristics, should depend on the specific dielectric or the dielectric deposition method. Yet, the reported admittance characteristics of well-behaved dielectric/III-V interfaces with different dielectrics and/or dielectrics deposited by different methods are remarkably similar.[5,15,24] The similarity in the observed characteristics of MOSCAPs in the literature is in keeping with a large body of work on III-V Schottky barriers and surfaces that have shown that semiconductor surface Fermi level pinning is largely caused by defects in the III-V semiconductor and not by the specific surface adsorbate or metal.[3,4] While these results point to semiconductor defects as the origin, the mechanisms by which they could cause frequency dispersion in accumulation are not understood. In this letter, we discuss a mechanism by which interface traps can give rise to strong frequency dispersion in accumulation for scaled III-V MOSCAPs. We show that this mechanism is consistent with the measured admittance characteristics and with the high-density and non-uniform trap distribution within the band gap that is typical for many III-V semiconductors.

In addition to communicating with the semiconductor bands, interface traps may communicate with the metal via tunneling, provided that the dielectric is thin.[25,26] The process by communication with the metal can give rise to a frequency-dependent ac conductance is schematically illustrated in Fig. 2 for positive gate bias and an *n*-type semiconductor that has a peak in D_{it}, as indicated. Specifically, for dielectrics on $In_{0.53}Ga_{0.47}As$, the D_{it} near midgap becomes very large.[5,6,15,24] At sufficient positive gate bias, the metal Fermi level will thus align with the high density of traps and electrons can tunnel from the traps to the metal. The ac signal causes the metal Fermi level (E_{Fm}) to oscillate through E_t (trap level). A conducting channel (ac loss) is provided through recombination of carriers with the interface states, as indicated by the vertical arrow in Fig. 2. When the tunneling time constant is small compared to the surface recombination time,[26] the process is known as "recombination-controlled tunneling." For traps that communicate with the conduction band, the ac conductance at a given applied bias, V_a, is given by[25]

$$G(V_a) = \frac{\omega^2\tau^2}{1+\omega^2\tau^2}\frac{dJ}{dV}\bigg|_{V_a}, \tag{1}$$

where J is the tunnel current density. The recombination time constant τ is proportional to the inverse of the semiconductor sheet carrier concentration, n_s,[25,26]

$$\tau = \frac{1}{\sigma\langle v\rangle(n_1+n_s)}, \tag{2}$$

where σ is the trap cross-section, $\langle v\rangle$ is the thermal velocity of the carriers, and the carrier concentration n_1 enters to balance the capture rate equations (see Ref. 26 for the derivation of Eq. (2); in accumulation n_1 is small compared to n_s). From Eq. (1), it can be seen that the conductance due to recombination-controlled tunneling is zero at dc and increases to dJ/dV as the frequency increases. Qualitatively, the observed conductance characteristics [Fig. 1(b)] agree with this. In addition, the model explains the fact that the dispersion becomes large at large positive biases, when the metal Fermi level faces the region where the D_{it} is high. For example, the dispersion in the capacitance for well-behaved MOSCAPs is relatively low at small positive bias and then increases with positive bias, as can be seen for example in Fig. 1(a). Given the doping and the flatband voltage (~0.4 V for the MOSCAP with 3 nm Al_2O_3), the metal Fermi level aligns with trap states near midgap at a gate bias around 1 V. Thus, it is likely that the same midgap traps that cause the frequency dependent "hump" in capacitance at negative bias, when these trap states align with the semiconductor Fermi level, are also responsible for the frequency dispersion in accumulation, when they align with the metal Fermi level. This also explains experimental results that show *simultaneous* reduction in dispersion in accumulation and depletion upon annealing.[8,23,27]

To determine if the observed frequency dispersion in accumulation can be described quantitatively by the recombination-controlled tunneling mechanism, normalized plots of G_p/ω versus log frequency are shown in Figs. 3(a) and 3(b)). Referring again to Eq. (1), these should exhibit a maximum at $\omega\tau \approx 1$. Figures 3(a) and 3(b) show that the G_p/ω versus log frequency at different positive gate biases for the MOSCAPs of Figs. 1(a) and 1(b) exhibit maxima. The dashed line in Fig. 3(a) shows that these maxima can be described by a function of form $\omega\tau^2/(1+\omega^2\tau^2)$, as predicted by Eq. (1). The theoretical function is symmetric, while the experimental curve falls off less rapidly with frequency. For the conventional mechanism of communication

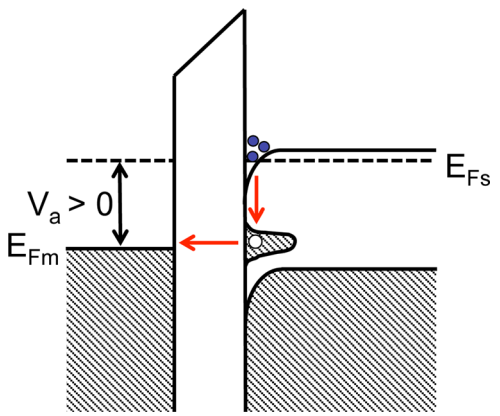

FIG. 2. Energy-band diagram of an *n*-channel MOSCAP in accumulation. A peak in the interface trap state density is shown. The arrows indicate a recombination-controlled tunneling process, involving tunneling (horizontal arrow) and electron capture processes. E_{Fm} and E_{Fs} indicate the metal and semiconductor Fermi levels, respectively.

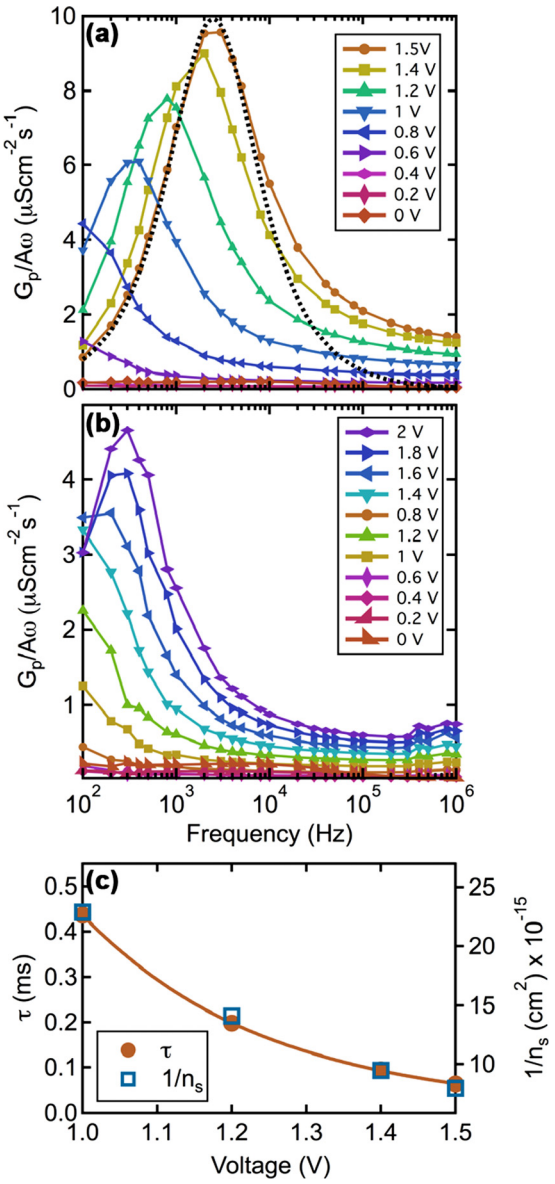

FIG. 3. G_p/ω versus log frequency curves for (a) 3 nm thick Al_2O_3/$In_{0.53}Ga_{0.47}As$ and (b) 5 nm thick Al_2O_3/$In_{0.53}Ga_{0.47}As$. The black dotted line in (a) is a plot of the function $C\omega\tau^2/(1+\omega^2\tau^2)$, where C is a constant. (c) Plot of extracted τ parameters (left axis) as a function of voltage for the 3 nm thick Al_2O_3/$In_{0.53}Ga_{0.47}As$ sample obtained from fitting the G_p/ω plots to Eq. (1). The solid line is an exponential fit to the data. Also shown is the inverse of the estimated semiconductor sheet carrier density (right axis).

with the bands, this has been attributed to fluctuations in the surface potential.[13] Another possibility is contribution from a series resistance term at high frequencies. For the MOSCAP with the thicker dielectric [Fig. 3(b)], larger positive gate biases are needed to observe the peak, as expected due to the reduced capacitance density of this stack (see discussion of τ below). The tunnel conductance extracted using the peaks (see Eq. (1)) is a factor of ~14 higher for the 3 nm Al_2O_3 (at 1.4 V) than for the 5 nm (at 1.8 V). The increase agrees with estimates based on Wentzel, Kramers, and Brillouin (WKB) theory of the thickness dependence of the tunneling current. The fact that a discrete peak is observed in Figs. 3(a) and 3(b) indicates that the conductance experiment probes a discrete trap state, rather than a wide distribution of states.[25] From fits of the experimental data to Eq. (1), shown in Fig. 3(c), it can be seen that the trap time constant, τ, exponentially decreases with applied bias. This agrees with Eq. (2), i.e., τ is inversely proportional to the semiconductor surface charge density, n_s.[13,25] Specifically, the estimated inverse of the charge density, $(n_s)^{-1}$ for this MOSCAP,[17] also shown in Fig. 3(c), and τ have a similar dependence on the applied voltage. We note that the standard model for the conductance through communication with the semiconductor bands,[13] i.e., in the absence of tunneling, also gives rise to a G_p/ω peak, but for the reasons discussed above, no frequency dispersion is expected in accumulation due to this mechanism. Border traps should not result in a G_p/ω peak.[13]

An important consideration is the contribution from frequency-independent band-to-band tunneling to the measured conductance, which dominates for Si MOSCAPs with thin dielectrics.[28,29] As can be seen from Fig. 1(b), for the III-V MOSCAP, the largest contribution to the conductance at positive gate biases is strongly frequency dependent. Dielectric/III-V interfaces differ in two important aspects from SiO_2/Si interfaces: (i) the D_{it} of dielectric/III-V interfaces is orders of magnitude higher than for Si MOSCAPs (rising well into $10^{14}\,eV^{-1}cm^{-2}$ near the valence band[24]), allowing for a large tunnel current through these states and (ii) the conduction band DOS of III-V semiconductors such as $In_{0.53}Ga_{0.47}As$ is several orders of magnitude lower than that of Si. As a result, the surface charge density, which determines band-to-band tunneling, remains around $10^{13}\,cm^{-2}$.[15] Although there is currently no complete theory describing the tunneling current for extremely high-density of interface states, the large ratio of D_{it} relative to conduction band DOS will make tunneling through interface states a significant contribution to the total conductance of III-V MOSCAPs.

In summary, we have shown that the frequency dispersion in accumulation of typical dielectric/*n*-$In_{0.53}Ga_{0.47}As$ MOSCAPs, the appearance of a G_p/ω peak at positive gate bias, and the thickness dependence of the conductance are consistent with the communication of a high density of interface traps with the metal. The interface trap states that are responsible for the frequency dispersion in accumulation reside in the *lower half of the $In_{0.53}Ga_{0.47}As$ band gap*, as the metal Fermi level lines up with these states only at positive gate biases. The strong frequency dispersion is thus directly a consequence of the asymmetric (with respect to their position in the band gap) distribution of trap states in semiconductors such as $In_{0.53}Ga_{0.47}As$. We note that more extreme forms of dispersion are seen in cases of pinned interfaces and thick dielectrics (such as for p-$In_{0.53}Ga_{0.47}As$, see, i.e., Ref. 15); in such cases, accumulation is not reached and the mechanisms discussed here do not apply. The most important practical consequence of the recombination-controlled tunneling processes is that for n-type channels not only must trap densities in the upper half of the band gap be sufficiently low (to enable efficient semiconductor band bending for MOSFET operation) but, to achieve low frequency dispersion with thin dielectrics, trap states in the lower half of the band gap must also be controlled. For $In_{0.53}Ga_{0.47}As$, reducing the midgap trap densities has proven to be very challenging. Finally, we note that the communication of the trap

states with the metal must also be included in the analysis of interface traps in depletion and weak inversion regions, which will be the subject of future work.

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