High Performance 0.1 μm Gate-Length P-Type SiGe MODFET's and MOS-MODFET's

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***Abstract*—High performance p-type modulation-doped field-effect transistors (MODFET's) and metal-oxide semiconductor MODFET (MOS-MODFET) with 0.1 μm gate-length have been fabricated on a high hole mobility SiGe/Si heterojunction grown by ultrahigh vacuum chemical vapor deposition. The MODFET devices exhibited an extrinsic transconductance (g_m) of 142 mS/mm, a unity current gain cut-off frequency (f_T) of 45 GHz and a maximum oscillation frequency ($f_{\rm MAX}$) of 81 GHz. 5 nm-thick high quality jet-vapor-deposited (JVD) SiO_2 was utilized as gate dielectric for the MOS-MODFET's. The devices exhibited a lower gate leakage current (1 nA/μm at $V_{gs} = 6$ V) and a wider gate operating voltage swing in comparison to the MODFET's. However, due to the larger gate-to-channel distance and the existence of a parasitic surface channel, MOS-MODFET's demonstrated a smaller peak g_m of 90 mS/mm, f_T of 38 GHz, and $f_{\rm MAX}$ of 64 GHz. The threshold voltage shifted from 0.45 V for MODFET's to 1.33 V for MOS-MODFET's. A minimum noise figure ($\rm NF_{min}$) of 1.29 dB and an associated power gain (G_a) of 12.8 dB were measured at 2 GHz for MODFET's, while the MOS-MODFET's exhibited a $\rm NF_{min}$ of 0.92 dB and a G_a of 12 dB at 2 GHz. These dc, rf, and high frequency noise characteristics make SiGe/Si MODFET's and MOS-MODFET's excellent candidates for wireless communications.**

***Index Terms*—MODFET, MOS-MODFET, silicon–germanium.**

I. Introduction

RECENT advances in the growth and processing of p-type and n-type SiGe modulation-doped field effect transistors (MODFET) have resulted in devices with excellent dc and rf characteristics [1]–[6]. To improve the performance of complementary metal-oxide-semiconductor (CMOS) circuits, attempts also have been made to fabricate high performance p-type metal-oxide-semiconductor field-effect transistors on modulation-doped SiGe heterostructures (MOS-MODFET) [7]–[10]. However, the progress made in realizing high performance SiGe MOSFET's has been limited. This is due to a number of factors which include high density of interface states of oxides formed on SiGe, Ge segregation caused by high temperature oxide processing, and the effects of alloy and intersubband scattering. Overall, SiGe MOSFET's have not realized the potential predicted by theory [11]. Recently, we reported a 0.25 μm MOS-MODFET for which jet-vapor-deposited (JVD) silicon nitride [12] was used as gate dielectric that exhibited a transconductance of 167 mS/mm, a unity current gain cut-off frequency (f_T) of 27 GHz, a maximum oscillation frequency ($f_{\rm MAX}$) of 45 GHz [13]. These p-type SiGe MOS-MODFET's with gate-lengths ranging from 0.25 μm to 1.0 μm demonstrated much smaller gate leakage currents and better pinch-off characteristics in comparison with conventional MODFET's. However, as expected, threshold voltages of MOS-MODFET's increased because of the existence of the gate dielectric layer. Conventional MODFET's suffer from a reduced gate voltage swing due to the onset of a significant leakage current across the Schottky gate under forward bias condition. Therefore the exploration of devices with wider gate voltage swings and low leakage currents is of significant interest. The insertion of gate dielectrics between the gate and the semiconductor does suppress leakage currents but it brings about other problems such as the formation of parasitic surface channels. Therefore, investigations on MOS-MODFET's especially at shorter gate lengths are required for detailed comparison with MODFET's. In this paper, a systematic comparative study of p-type SiGe/Si MODFET's and MOS-MODFET's with 0.1 μm gate-length have been performed. This paper is organized as follows. The structure and fabrication of devices are described in Section II. Section III presents the dc , rf, and high frequency noise results and discussion of fabricated MODFET's and MOS-MODFET's. Finally, some conclusions are drawn in Section IV.

II. Device Structure and Fabrication

The SiGe/Si heterostructure layer was grown by ultra-high vacuum chemical vapor deposition (UHV-CVD) on an n^-Si substrate. The layer sequence started with a linearly step-graded $Si_{(1-x)}Ge_x$ buffer layer relaxed to the lattice constant of $Si_{0.7}Ge_{0.3}$. A 1 μm-thick $Si_{0.7}Ge_{0.3}$ buffer layer was followed by the modulation-doped structure which consisted of a 4-nm B-doped $Si_{0.7}Ge_{0.3}$ supply layer at a doping density of 2×10^{18} cm^{-3}, a 3-nm undoped $Si_{0.7}Ge_{0.3}$ spacer, and a 4.5 nm-thick $Si_{(1-x)}Ge_x$ channel graded from 0.8 to 0.7, and a 10 nm $Si_{0.7}Ge_{0.3}$ cap layer. The layer exhibited a 2-D hole-gas mobility of 930 cm^2/Vs and a hole sheet density of 2.6×10^{12} cm^{-2} as determined by Hall measurements at room temperature.

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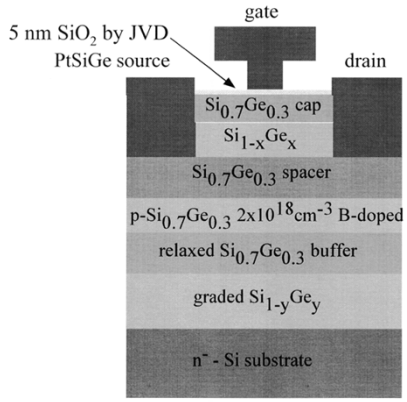


Fig. 1. Cross-sectional schematic of the UHV-CVD grown p-type SiGe MOS-MODFET heterostructure.

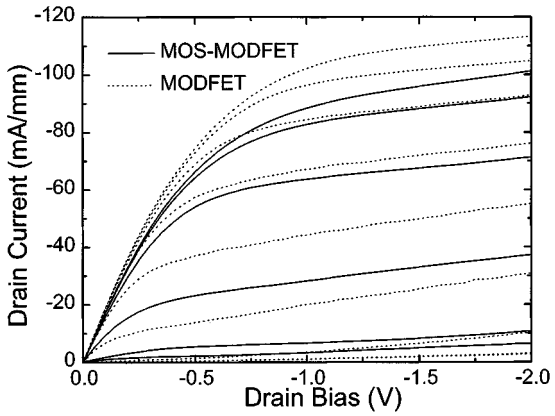


Fig. 2. Room temperature *I–V* characteristics of a typical 0.1 μm gate length p-type MODFET and MOS-MODFET with a 100-μm gate width. The gate bias was swept from -0.6 V to 0.8 V in a step of 0.2 V for the MODFET and from -0.5 V to 2.0 V in a step of 0.5 V for the MOS-MODFET.

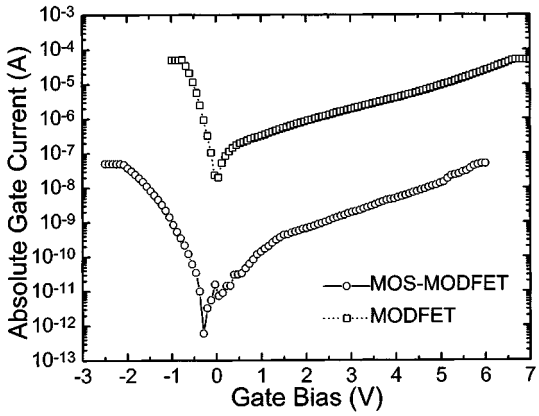


Fig. 3. Comparison of Schottky characteristics of a 0.1 μm MODFET and the gate leakage current of a 0.1 μm MOS-MODFET with same 50 μm gate width at $V_{ds} = 0$ V.

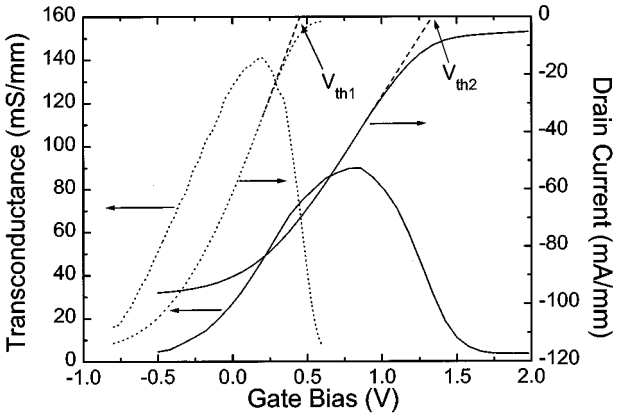
The processing of MOS-MODFET's started with the deposition of a 5-nm-thick SiO_2 film using the JVD method. The details of the equipment and the process are described elsewhere [12]. To densify the film, the sample received a post-deposition annealing at 300 °C in nitrogen ambient for 30 min. Mesa isolation was achieved using reactive ion etching in a CF_4 plasma. The mesa height was 170 nm. The sample was passivated using 240-nm-thick electron beam-evaporated SiO_2 film. The ohmic metallization of 30-nm-thick Pt was evaporated and lifted-off after the oxide in the ohmic area was removed by wet chemical etching. A contact resistance of $\sim$0.2–0.3 Ω-mm was obtained after the sample was sintered in a nitrogen ambient at 350 °C for 5 min. The mushroom Ti/Pt/Au gates with 0.1 μm gate length were patterned with a trilayer resist system using electron beam lithography. Finally, the contact pads were defined by deposition of Ti/Pt/Au. The source-drain distance was 2 μm while the gate width of all devices was 100 μm with two fingers in a T-configuration. The device structure of MOS-MODFET's is shown in Fig. 1. Conventional MODFET's were simultaneously fabricated on another sample with the same structure but without the JVD oxide. The processing of MODFET's was similar to the processing of the MOS-MODFET's. Prior to gate and ohmic metallizations on the MODFET's, native oxide was removed by a dip in dilute HF.

III. Device Performance and Discussion

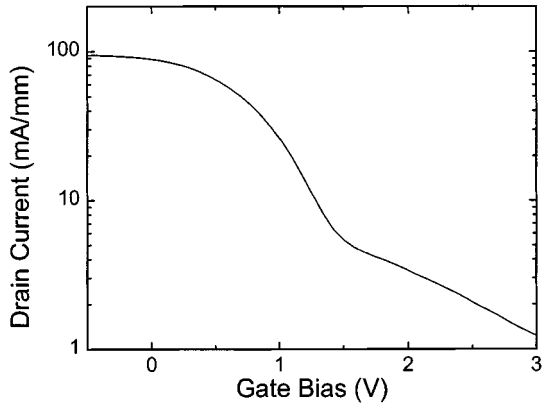
A. DC Characteristics

On-wafer dc measurements were performed on the devices using a Cascade Microtech Probe station and an HP4145 Semiconductor Parameter Analyzer. Fig. 2 shows the I_{ds}–V_{ds} characteristics of a typical MOS-MODFET and a MODFET with a gate length of 0.1 μm. The MODFET shows excellent pinch-off characteristics at $V_{gs} = 0.8$ V with an off-state current of 1.0 mA/mm at $V_{ds} = -1.0$ V, resulting in a low off-state power consumption. Surprisingly, unlike the earlier results [13] of our MOS-MODFET's with $0.25 \sim 1.0$ μm gate-lengths, MODFET's have better pinch-off characteristics than MOS-MODFET's. The off-state current is 3.2 mA/mm at $V_{ds} = -1.0$ V and $V_{gs} = 2.0$ V. The larger gate-to-channel distance of the MOS-MODFET's shifts the threshold voltage toward the positive direction. As a result, the pinch-off voltage of MOS-MODFET's is as high as 2 V. With this gate bias, a surface channel seems to have been formed and turned-on. This type of behavior has been theoretically predicted by Verdonckt–Vandebroek *et al.* [7], [14] and will be discussed later. The maximum drain current of the MODFET measured in the saturation regime is 114 mA/mm at $V_{gs} = -0.6$ V and $V_{ds} = -2.0$ V. The MOS-MODFET has a slightly lower drain drive current (102 mA/mm at $V_{gs} = -0.5$ V and $V_{ds} = -2.0$ V) due to the larger gate-to-channel distance caused by the insertion of JVD oxide gate dielectric layer, which degrades the modulation efficiency of devices. Both the MOS-MODFET and MODFET show relatively low knee voltages, which are 0.6 V.

Fig. 3 shows a comparison of the gate leakage currents of a MOS-MODFET with 0.1 μm gate-length and 50 μm gate-width and the Schottky characteristics of a MODFET with the same gate-length and gate-width. In these measurements, the drain was shorted to the source. For the MODFET, the turn-on voltage is 0.76 V and the gate-drain breakdown voltage is 6.7 V, using the definition of gate forward and reverse biases at the gate current of 1 mA/mm, respectively. For the MOS-MODFET, shown in Fig. 3, the gate leakage current is extremely small, at least three orders of magnitude smaller than that of MODFET's at the



(a)



(b)

Fig. 4. (a) Transfer characteristics of a 0.1 μm MOS-MODFET (solid lines) and a 0.1 μm MODFET (dot lines). The drain bias was -1.0 V for both the MODFET and the MOD-MODFET. The tangent lines are use to determine the threshold voltages. The threshold voltage shifts from 0.45 to 1.33 V after the insertion of a thin JVD oxide film between the gate and the cap layer. (b) Subthreshold drain current characteristics of the MOS-MODFET. The surface parasitic channel is turned-off slowly at the subthreshold region.

same reverse biases and five orders of magnitude smaller than that at the same forward biases. The forward and reverse gate biases are 2.16 V and 6.0 V, respectively, at the gate current level of 1 nA/μm, which is the industry standard for sub-threshold gate leakage current for high performance MOS transistors. This indicates that the quality of the JVD oxide gate dielectric layer is very high and that it safely fulfills the requirement of the gate operation range of the MOS-MODFET's.

The dc transfer characteristics of the same MOS-MODFET are shown in Fig. 4(a). For comparison, the transfer characteristics of the MODFET are also shown in Fig. 4(a). The drain bias was -1.0 V for both transistors. The results illustrated in Fig. 4(a) show the following.

1) At a gate bias of 0.2 V, the MODFET exhibits a maximum extrinsic transconductance (g_m) of 142 mS/mm. Not surprisingly, the MOS-MODFET exhibits lower peak extrinsic transconductance of 90 mS/mm at the gate bias of 0.86 V, because of the lower modulation efficiency caused by the larger gate-to-channel distance. It is reasonable to consider the relative permitivity of $Si_{(1-x)}Ge_x$ increases linearly with Ge mole fraction x. So, the equivalent thickness of the 5 nm SiO_2 gate dielectric layer relative to $Si_{0.7}Ge_{0.3}$ cap layer is, $t_{ox} \cdot \varepsilon_{\mathrm{Si0.7Ge0.3}}/\varepsilon_{ox} = 16.9$ nm. (In this calculation, $\varepsilon_{\mathrm{Si}}/\varepsilon_0 = 11.9$, $\varepsilon_{\mathrm{Ge}}/\varepsilon_0 = 16.1$, and $\varepsilon_{ox}/\varepsilon_0 = 3.9$, and $\varepsilon_{\mathrm{Si0.7Ge0.3}}/\varepsilon_0 = 13.16$.) Then, the total effective gate-to-channel distance for MOS-MODFET's is 26.9 nm while the gate-to-channel distance of MODFET's is only 10 nm. In comparison with the devices that we reported earlier with 0.25 μm gate-length [13], the g_m of these 0.1 μm devices is somewhat lower. However, the present devices exhibit better RF performances, as we will demonstrate later. This is attributed to the higher source access resistance because of the larger gate-to-source distance. From our Hall measurement results, the sheet resistance $R_{\mathrm{sheet}} = \mu n q = 2.58 \times 10^3\ \Omega$/square, where μ is the mobility, q is the electron charge, and n is the sheet carrier density. For a 0.1 μm-gate MODFET with 2 μm source drain spacing, the source access resistance $R_{acc} = R_{\mathrm{sheet}} \cdot L_{gs} = 2.45\ \Omega \cdot$ mm, assuming that the gate is centrally located between the source and drain. This is much higher than the ohmic contact resistance. So, the intrinsic transconductance of MODFET's mainly depends on the access resistance, $g_{mint} = g_{mext}/[1 - g_{mext}(R_c + R_{acc})] = 233.1$ mS/mm.
2) The g_m curve of the MODFET shows higher peak transconductance but a very sharp peak, corresponding to a small gate swing voltage. Though the MOS-MODFET has a lower peak transconductance, the g_m curve has a wider response with respect to V_{gs}. The full width at half maximum (FWHM) of the MODFET is 0.82 V while the FWHM of the MOS-MODFET is 1.08 V, which indicates a wider gate operation range. This improvement is not completely due to the lower transconductance but actually represents improved linearity. This will clearly be demonstrated in rf performances.
3) It is seen that the gate bias of peak transconductance is shifted from 0.2 to 0.86 V in the reverse bias direction, after the insertion of the ultrathin JVD oxide film. By defining the threshold voltage (V_{th}) as the gate bias intercept of the extrapolation of I_{ds} at the point of peak g_m, the threshold voltages of the MODFET and MOS-MODFET, V_{th1} and V_{th2} shown in Fig. 4, are 0.45 and 1.33 V, respectively. This is mainly due to the degraded modulation efficiency caused by the much larger equivalent gate-to-channel distance as we described earlier because of the much lower relative permitivity of silicon dioxide.
4) Unlike the devices with larger gate-lengths, the 0.1 μm MOS-MODFET pinched-off slowly at high gate biases. Again, this is mainly attributed to the lower modulation efficiency caused by the larger gate-to-channel distance. Another reason may be due to the lower mobilities of holes in the surface channel. Fig. 4(b) shows the subthreshold characteristics of the MOS-MODFET. In the subthreshold region, it is clearly shown that the surface channel slowly pinches-off. At the gate bias of 3 V, the drain current is 1.2 mA/mm. The purpose of SiGe cap layer between the channel layer and SiO_2 dielectric layer is to separate the SiGe channel from SiO_2 and to decrease

the interface state density. But with the introduction of the cap layer, a number of holes will travel in the thin cap layer and thus a parasitic surface channel is introduced. The number of holes in the cap layer should be minimized because holes in this layer have lower mobilities. We think that the relatively high pinch-off voltage of MOS-MODFET's is caused by the combined effects of poor hole mobility in the parasitic surface channel and the lower modulation efficiency resulting from the larger gate-to-channel distance. The hole mobility of parasitic surface channel is so low compared with the holes in the channel that the surface channel is pinched-off completely after the SiGe channel, though it turns-on initially. Mathew *et al.*observed a clear and separate g_m peak for the surface channel of a SiGe p-MOSFET operating at 85 K [15], which indicated the turn-on of the surface channel and the resulting increase in the effective charge control capacitance. In this work, the separate g_m peak is not apparent because the transition of charge control capacitance at the onset of surface-channel is much less abrupt [14]. The high pinch-off voltage problem should become even more severe as gate length shrinks to less than 100 nm. In that case, threshold voltage adjustment is required to push the V_{th} into forward direction. Currently, we are investigating the possibility of depositing the gate dielectric layer directly on the channel layer without a cap layer. This is because we believe that the interface-trap density will be low enough between our JVD SiO_2 and the $Si_{(1-x)}Ge_x$ channel. By eliminating the cap layer, the transconductance should be higher, and also the parasitic surface channel will be eliminated.

B. RF Characteristics

For rf characteristics, on-wafer measurements of S-parameters from 1–35 GHz using a Cascade Microtech Probe and an HP8510B Network Analyzer have been used to determine unity current gain cut-off frequencies (f_T) and maximum oscillation frequencies ($f_{\rm MAX}$) of MODFET's and MOS-MODFET's. The current gain $|h_{21}|$, the maximum stable power gain (MSG) and the maximum available power gain (MAG) of a typical MODFET and a MOS-MODFET are plotted against frequency in Fig. 5. The f_T and $f_{\rm MAX}$ were obtained by the extrapolation of $|h_{21}|$ and MAG using a -20 dB/decade slope. At a drain bias of -0.9 V and a gate bias of 0.2 V, the MODFET exhibits an f_T of 45 GHz and an $f_{\rm MAX}$ of 57 GHz. The MOS-MODFET shows a lower f_T of 38 GHz, but only slightly lower $f_{\rm MAX}$ (55 GHz) than the MODFET at the same drain bias of -0.9 V and a gate bias of 0.8 V. The f_T and $f_{\rm MAX}$ values as functions of gate bias for the MODFET and MOS-MODFET are shown in Fig. 6 at a drain bias of -0.9 V. It is observed that the MODFET demonstrates higher peak f_T and $f_{\rm MAX}$. As we mentioned earlier, the disadvantage for MODFET's is the limited gate logic swing. Despite the lower transconductance of MOS-MODFET's, the value of V_{gs} for which $f_T > 30$ GHz is clearly wider, from 0.3 to 1.4 V for MOS-MODFET's and from -0.2 to 0.45 V for MODFET's. This confirms that the increased voltage swing of the MOS-MODFET's is not, at least not completely, due to the lower transconductance but actually

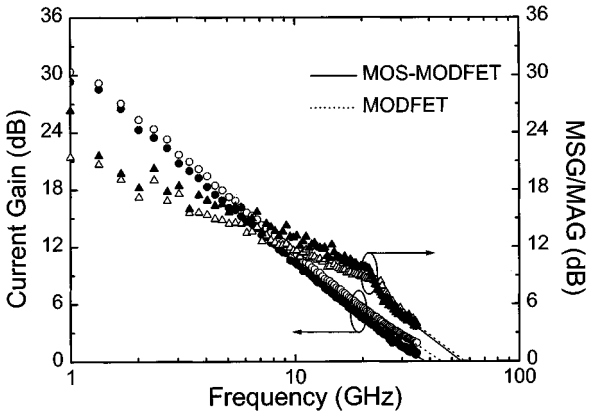


Fig. 5. Measured current gain ($|h_{21}|$), maximum stable gain (MSG) and maximum available gain (MAG) versus frequency for a typical 0.1 μm MOS-MODFET (solid symbols and lines) and a 0.1 μm MODFET (open symbols and dashed lines) with 100 μm gate-width. The MODFET was biased at $V_{ds} = -0.9$ V and $V_{gs} = 0.2$ V and the MOS-MODFET was biased at $V_{ds} = -0.9$ V and $V_{gs} = 0.8$ V.

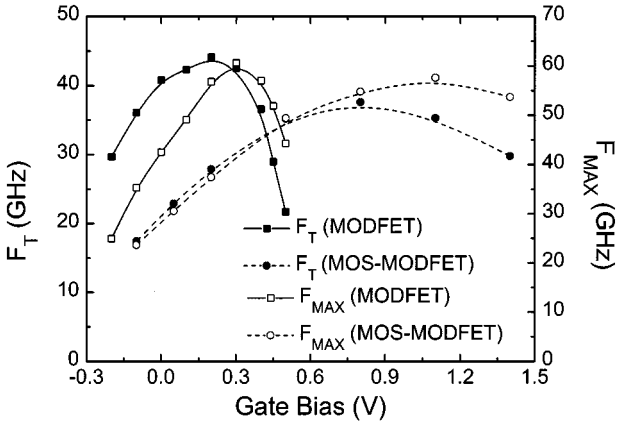


Fig. 6. Measured unity current gain cut-off frequency (f_T) and maximum oscillation frequency ($f_{\rm MAX}$) as a function of gate biases of a typical 0.1 μm MOS-MODFET and a 0.1 μm MODFET with 100 μm gate-width. The drain bias was -0.9 V for both transistors.

represents improved linearity. Actually, the smaller gate capacitance plays an important role also. Due to the presence of gate oxide in MOS-MODFET's, the input gate capacitance is clearly smaller if we consider the oxide and SiGe cap layer as a series of capacitors. The lower gate input capacitance results in higher f_T. So, we conclude that the improved linearity is due to the presence of the gate oxide layer which results in lower capacitance and lower transconductance. Fig. 7 shows f_T and $f_{\rm MAX}$ dependence on drain bias for the same devices measured above. The gate biases for the MODFET and MOS-MODFET are 0.3 V and 0.8 V, respectively. With increasing drain bias, for both MODFET and MOS-MODFET, f_T values do not change while $f_{\rm MAX}$ values slightly increase. For the MODFET, $f_{\rm MAX}$ saturates at 81 GHz at a drain bias of -1.9 V. For the MOS-MODFET, $f_{\rm MAX}$ saturates at 64 GHz at a drain bias of -1.8 V.

C. High Frequency Noise Performances

Transistor noise performance, which can be virtually ignored in digital systems, is an important issue in rf and microwave

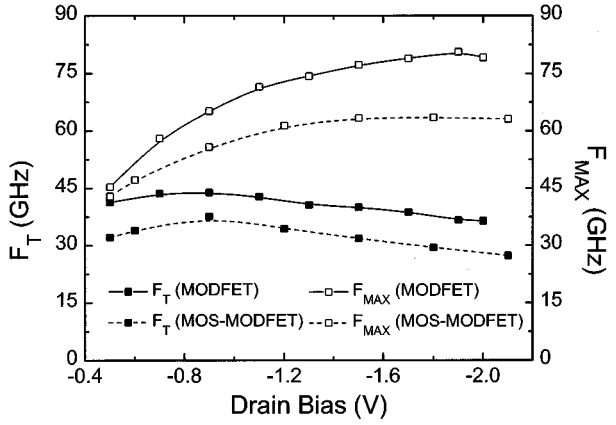


Fig. 7. Measured unity current gain cut-off frequency (f_T) and maximum oscillation frequency ($f_{\rm MAX}$) as a function of drain biases of a 0.1 μm MOS-MODFET and a 0.1 μm MODFET with 100 μm gate-width. The gate biases were 0.3 V and 0.8 V for the MODFET and the MOS-MODFET, respectively.

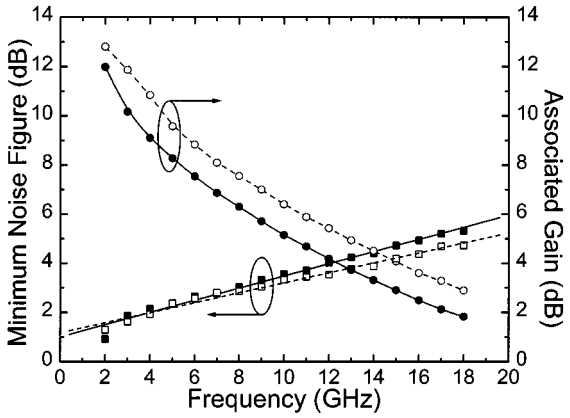


Fig. 8. Minimum noise figure and associated gain versus frequency of a typical 0.1 μm MOS-MODFET and a 0.1 μm MODFET with 100 μm gate-width. The MOS-MODFET was biased at $V_{ds} = -0.9$ V and $V_{gs} = 0.9$ V. The bias conditions for the MODFET are $V_{ds} = -0.9$ V and $V_{gs} = 0.3$ V.

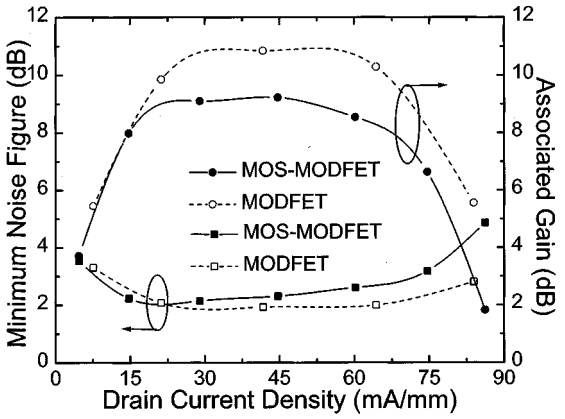


Fig. 9. Dependence of minimum noise figure and associated gain at 4 GHz on the current density of a typical 0.1 μm MOS-MODFET and a 0.1 μm MODFET with 100 μm gate-width. The drain bias was -0.9 V for both devices.

communications system design. High frequency noise performances of transistors play a major role in system sensitivity since it sets signal-to-noise level on low noise amplifiers used in front-end circuits for system applications. High frequency noise performance was measured using an HP8510B Network Analyzer and an ATN NP5 noise parameter test set over 2–18 GHz frequency range. After the system is calibrated, the uncertainties in the minimum noise figure ($\rm NF_{min}$) [16] and the associated power gain (G_a) [16] for standard "through" and "10 dB" passive structures were first measured to check the calibration. Repeated measurements for the same structure showed that the uncertainties of $\rm NF_{min}$ and G_a from 3 GHz up to 18 GHz are less than 0.1 dB. Since the NP5 noise measurement system does not peak the YIG at 2 GHz, it usually gives a higher uncertainty at 2 GHz. The $\rm NF_{min}$ at 2 GHz shown in this paper is actually the average of a number of repeated measurements at the same bias conditions. Fig. 8 shows $\rm NF_{min}$ and G_a of a 0.1 μm MOS-MODFET and a 0.1 μm MODFET as a function of frequency. In Fig. 8, the two straight lines are linear fits to the minimum noise figures. The bias conditions are $V_{ds} = -0.9$ V, V_{gs} =0.3 V for the MODFET and $V_{ds} = -0.9$ V, V_{gs} =0.9 V for the MOS-MODFET, respectively. At 2 GHz, the MODFET exhibited an $\rm NF_{min}$ of 1.29 dB and a G_a of 12.8 dB. The MOS-MODFET showed an $\rm NF_{min}$ of 0.92 dB and a G_a of 12.0 dB at 2 GHz. In general, for devices with 0.1 μm gate-length, at the frequency range of 2 to 8 GHz, MOS-MODFET's exhibited equal or even smaller $\rm NF_{min}$ than MODFET's, though the latter have higher G_a. But at higher frequency range, from 8–18 GHz, MODFET's exhibited lower $\rm NF_{min}$. Generally, the minimum noise figure of FET's can be estimated [18] by

$$\begin{aligned}\rm NF_{min} &= 10 \cdot \rm Log\left[1 + K_f \cdot f_M/f_T \cdot \{g_m(R_g + R_s)\}^{1/2}\right] \\ &= 10 \cdot \rm Log\left[1 + 2\pi \cdot K_f \cdot f_M(C_{gs} + C_{gd})\right. \\ &\quad \left.\cdot (R_g + R_s)^{1/2}/g_m^{1/2}\right] \end{aligned} \tag{1}$$

where K_f is Fukui factor and f_M is the operation frequency. The values of $g_m^{1/2}/f_T$ for the MOS-MODFET and the MODFET are 2.52×10^{-3} $\rm S^{1/2}$/GHz and 2.74×10^{-3} $\rm S^{1/2}$/GHz, respectively. It seems that MOS-MODFET's should exhibit a somewhat better noise performance. However, our results showed that MODFET's exhibited lower $\rm NF_{min}$ at $f_M > 8$ GHz. In the equivalent noise model, the Fukui factor can be expressed as [17],

$$K_f = 2\left\{P^{1/2} - R^{1/2} \cdot C_g/C_{11}\right) \tag{2}$$

where P and R numerical factors associated with the drain and gate thermal noise generators. But actually it is difficult to determine the Fukui factor quantitatively. However the measured higher $\rm NF_{min}$ at higher frequency indicates that the Fukui factor should be higher for MOS-MODFET's.

Fig. 9 shows the dependence of $\rm NF_{min}$ and G_a at 4 GHz on the drain current density, I_{ds}, which is controlled by the gate bias. The drain bias is -0.9 V for both the MODFET and the MOS-MODFET. From Fig. 9, comparing the two devices, the MODFET showed higher G_a and slightly lower $\rm NF_{min}$. A minimum noise figure of 1.9 dB at 4 GHz was measured for the MODFET and 2.1 dB was measured for the MOS-MODFET. Both the MODFET and the MOS-MODFET show very flat $\rm NF_{min}$ for a large range (15 mA/mm $\sim$ 70 mA/mm) of drain

current density. Comparatively, MOS-MODFET's show relative larger flat G_a range, while MODFET's have higher G_a.

It should be pointed out that these high frequency noise results are not as low as those achieved in GaAs-based MESFET's [18] and HEMT's [19]. If we assume that SiGe devices and GaAs-based devices with the same gate-lengths have similar gate capacitances (the relative permitivities of SiGe and GaAs are close) and gate and source resistances, the better noise figures of III–V devices are due to higher transconductance. This should be attributed to the higher electron mobility, better carrier confinement of heterojunction, and better modulation efficiency of GaAs-based heterostructures. On the other hand, the material quality of SiGe heterostructures is improving rapidly. So, better noise performance from SiGe devices should be expected in the future. Nevertheless, our results are comparable to or better than any reported results obtained for state-of-the-art Si-based devices. For example, Johnson *et al.* [20] reported 0.5 μm CMOS on sapphire low noise transistors, in which n-MOS transistors exhibited 1.1 dB $\mathrm{NF_{min}}$ and p-MOSFET's exhibited 0.9 dB $\mathrm{NF_{min}}$ at 2 GHz. Saito *et al.* [21] reported 0.15 μm RF CMOS on Si substrate with 1.4 dB $\mathrm{NF_{min}}$ at 2 GHz for n-MOSFET's and 2.8 dB at 2 GHz for p-MOSFET's. Ansley *et al.* [22] reported a SiGe HBT with 0.7 dB $\mathrm{NF_{min}}$ at 2.5 GHz. Clearly, the noise performance of the devices investigated in this work demonstrates their potentials in several radio frequency applications, such as mobile telecommunications. Moreover, these noise characteristics were measured without de-embedding the parasitic effects of pad losses. Parasitic losses of the pads substantially influence noise performance. The applications of silicon-on-insulator (SOI) technologies to SiGe MODFET's, better material quality, optimization of pad structures, and wider-head T-shaped gates for achieving lower gate resistances are expected to improve the high frequency minimum noise figure performances.

IV. Conclusions

The fabrication and characterization of 0.1 μm p-type SiGe MODFET's and MOS-MODFET's have been described. For the MODFET's, a maximum transconductance of 142 mS/mm, a maximum drain current of 114 mA/mm, and a gate to drain breakdown voltage of 6.7 V were achieved. An f_T of 45 GHz and an f_{MAX} of 81 GHz have been measured. For MOS-MODFET's, high quality ultrathin JVD oxide was used as gate dielectric layer. Using this approach, the MOS-MODFET's exhibited very small gate leakage current (less than 1 nA/μm in the gate bias range of -2.16 V to 6.0 V) and wide gate voltage swing. But with the introduction of the gate dielectric layer, a parasitic surface channel in the cap layer was introduced and was completely turned-on at about 2 V. As a result, the MOS-MODFET's have higher pinch-off voltages. The threshold voltage shifts from 0.45 V for MODFET's to 1.33 V for MOS-MODFET's. Due to the lower modulation efficiency caused by the longer gate-to-channel distance, MOS-MODFET's demonstrated a peak g_m of 90 mS/mm, f_T of 38 GHz, and f_{MAX} of 64 GHz. These are slightly lower than those obtained for MODFET's due to the reasons stated above. The advantages for MOS-MODFET's include smaller gate leakage current, wider gate voltage operation swing, and better device linearity. The f_T and f_{MAX} values reported for these devices are the highest so far for any p-type SiGe heterojunction nonself-aligned MOSFET's. In addition, for the first time, high frequency noise performances of SiGe FET's were investigated and reported. For the MODFET's, an $\mathrm{NF_{min}}$ of 1.29 dB and a G_a of 12.8 dB were measured at 2 GHz as well as an $\mathrm{NF_{min}}$ of 1.9 dB at 4 GHz. The MOS-MODFET's exhibited an $\mathrm{NF_{min}}$ of 0.92 dB and a G_a of 12 dB at 2 GHz and an $\mathrm{NF_{min}}$ of 2.1 dB at 4 GHz. All these attractive dc, rf, and high frequency noise characteristics indicate potential applications of SiGe/Si MODFET's and MOS-MODFET's in wireless communications. Further improvements on device performances are expected by the application of SOI technologies and by developing a self-aligned process, which would reduce the effect of the source access resistance and the source-drain transit delay.

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References

[1] K. Ismail *et al.*, "High-transconductance n-type Si/SiGe modulation-doped field-effect transistors," *IEEE Electron Device Lett.*, vol. 13, pp. 229–231, May 1992.

[2] M. Arafa *et al.*, "DC and RF performance of 0.25 μm p-type SiGe MODFET," *IEEE Electron Device Lett.*, vol. 17, pp. 449–451, Sept. 1996.

[3] M. Arafa *et al.*, "A 70-GHz f_T low operating bias self-aligned p-type SiGe MODFET," *IEEE Electron Device Lett.*, vol. 17, pp. 586–588, Dec. 1996.

[4] I. Adesida *et al.*, "Submicrometer p-type SiGe modulation-doped field-effect transistors for high speed applications," *Microelectron. Eng.*, vol. 35, pp. 257–260, 1997.

[5] M. Glück *et al.*, "High f_{MAX} n-type Si/SiGe MODFETs," *Electron. Lett.*, vol. 33, pp. 335–337, 1997.

[6] G. Höck *et al.*, "High performance 0.25 μm p-type Ge/SiGe MODFETs," *Electron. Lett.*, vol. 34, pp. 1888–1889, 1998.

[7] S. Verdonckt-Vandebroek *et al.*, "High-mobility modulation-doped graded SiGe-channel p-MOSFET's," *IEEE Electron Device Lett.*, vol. 12, pp. 447–449, Aug. 1991.

[8] E. Murakami, K. Nakagawa, A. Nishida, and M. Miyao, "Fabrication of a strain-controlled SiGe/Ge MODFET with ultrahigh hole mobility," *IEEE Trans. Electron Devices*, vol. 41, pp. 857–861, May 1994.

[9] B. Bhaumik *et al.*, "23 GHz room temperature SiGe quantum well p-MOSFETs," in *Proc. 1993 Int. Semiconductor Device Res. Symp.*, Charlottesville, VA, 1993, pp. 349–352.

[10] K. Rim, J. Welser, J. L. Hoyt, and J. F. Gibbons, "Enhanced hole mobilities in surface-channel strained-Si p-MOSFETs," in *IEDM Tech. Dig.*, 1995, pp. 517–520.

[11] A. G. O'Neill and D. A. Antoniadis, "Deep submicron CMOS based on silicon germanium technology," *IEEE Trans. Electron Devices*, vol. 43, pp. 911–918, June 1996.

[12] T. P. Ma, "Making silicon nitride film a viable gate dielectric," *IEEE Trans. Electron Devices*, vol. 45, pp. 680–690, Mar. 1998.

[13] W. Lu *et al.*, "p-type SiGe transistors with low gate leakage using SiN gate dielectric," *IEEE Electron Device Lett.*, vol. 20, pp. 514–516, Oct. 1999.

[14] S. Verdonckt-Vandebroek *et al.*, "SiGe-channel heterojunction p-MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, pp. 90–101, Jan. 1994.

[15] S. J. Mathew *et al.*, "Hole confinement and low-frequency noise in SiGe pFET's on silicon-on-sapphire," *IEEE Electron Device Lett.*, vol. 20, pp. 173–175, Apr. 1999.

[16] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*. Englewood Cliffs, NJ: Prentice-Hall, 1996, pp. 480–492.
[17] F. Ali and A. Gupta, *HEMT's and HBTs: Devices, Fabrication and Circuits*. Norwell, MA: Artech House, 1991, p. 70.
[18] K. Onodera, K. Nishimura, S. Aoyama, S. Sugitani, Y. Yamane, and M. Hirano, "Extremely low-noise performance of GaAs MESFET's with wide-head T-shaped gate," *IEEE Trans. Electron Devices*, vol. 46, pp. 310–319, Feb. 1999.
[19] J. H. Lee, H. S. Yoon, C. S. Park, and H. M. Park, "Ultra low noise characteristics of AlGaAs/InGaAs/GaAs pseudomorphic HEMT's with wide head T-shaped gate," *IEEE Electron Device Lett.*, vol. 16, pp. 271–273, Apr. 1995.
[20] R. A. Johnson *et al.*, "Advanced thin-film silicon-on-sapphire technology: Microwave circuit applications," *IEEE Trans. Electron Devices*, vol. 45, pp. 1047–1054, May 1998.
[21] M. Saito, M. Ono, R. Fujimoto, H. Tanimoto, N. Ito, T. Yoshitomi, T. Ohguro, H. S. Momose, and H. Iwai, "0.15 μm RF CMOS technology compatible with logic CMOS for low-voltage operation," *IEEE Trans. Electron Devices*, vol. 45, pp. 737–742, Mar. 1998.
[22] W. E. Ansley, J. D. Cressler, and D. M. Richey, "Base-profile optimization for minimum noise figure in advanced UHV/CVD SiGe HBT's," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 653–660, May 1998.

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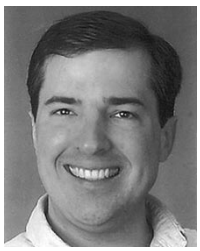

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