N-Face Metal–Insulator–Semiconductor High-Electron-Mobility Transistors With AlN Back-Barrier

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***Abstract*—We present a high-performance SiN/AlGaN (cap)/GaN (channel)/AlN (barrier)/GaN (buffer) metal–insulator–semiconductor high-electron-mobility transistor grown on the N-face, in which the 2-D electron gas (2DEG) is induced at the top GaN/AlN interface. The use of AlN eliminates alloy disorder scattering to the 2DEG and provides strong back-barrier confinement of the 2DEG under high electric fields for device scaling. Devices with 0.7-μm gate length showed a current-gain cutoff frequency (f_T) of 17 GHz and a power-gain cutoff frequency ($f_{\max}$) of 37 GHz. A continuous-wave output power density of 7.1 W/mm was measured at 4 GHz, with 58% power-added efficiency and a large-signal gain of 15.3 dB at a drain bias of 35 V.**

***Index Terms*—AlN, back-barrier, GaN, high-electron-mobility transistor (HEMT), N-face, metal–insulator–semiconductor (MIS).**

I. Introduction

RECENT advancements in materials growth and device technology have made gallium nitride an excellent candidate for wireless communication applications. The high breakdown voltage of the nitride material system, together with the development of field-plate and passivation technologies, has enabled devices with continuous-wave output power densities in excess of 40 W/mm at 4 GHz and 20 W/mm at 10 GHz [1], [2]. Aggressive reduction of the gate length down to sub-100 nm and the corresponding scaling of device aspect ratio have led to high intrinsic current- and power-gain cutoff frequencies (f_T and $f_{\max}$) of 190 and 251 GHz, respectively [3]. The realization of high power gain at millimeter-wave frequencies renders nitride-based high-electron-mobility transistors (HEMTs) attractive for power amplifier applications in the Ka-band and beyond.

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As the gate length of the devices decreases to allow for higher frequency of operation, increased confinement of the 2-D electron gas (2DEG) becomes important for maintaining the modulation efficiency of the gate in order to reduce short-channel effects such as soft pinchoff and high output conductance under high electric fields. Techniques using double heterostructures, such as wide-bandgap buffers [4]–[6] and InGaN back-barriers [7], were commonly employed to reduce current injection into the buffer by raising the conduction band edge in the buffer with respect to the channel. In addition, parasitic resistances limit the speed of highly scaled HEMTs. High resistances introduce noise while reducing the gain and efficiency of the devices. In Ga-face HEMTs, the wide-bandgap AlGaN barrier layer and its associated conduction band discontinuities with GaN have presented difficulties to realizing low contact resistances in Ga-face HEMTs [8].

An alternative approach to overcome the aforementioned challenges encountered as device dimensions decrease is by growing HEMT structures inverted on the N-face $(000\bar{1})$ orientation. N-face offers a few unique advantages for highly scaled devices. Due to the absence of inversion symmetry in wurtzite (Ga, Al, In)N, the polarization in N-face materials is opposite to that in III-face (0001) materials. This enables N-face heterojunction designs where the 2DEG forms above the wide-bandgap layer that acts as an inherent back-barrier. At the same time, the polarization in N-face materials allows device structures where the metal-to-2DEG connection does not need to go through a wide-bandgap AlGaN layer, offering the potential of achieving much lower ohmic contact resistances in N-face devices [8]. Moreover, the relative ease of growing high-quality N-face InGaN compared to In-polar growths has created new opportunities for exploring the use of high-velocity InGaN channel layers [9]. Although early researchers have suggested the inferior material quality and electrical properties of N-face heterostructures [10], [11], advances in growth on SiC have provided new opportunities for developing devices based on N-face materials [12], [13]. With extensive development of the growth and processing of N-face transistors [14], room-temperature 2DEG mobility exceeding 1700 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ and an output power density of 4.5 W/mm at 4 GHz have been achieved [15]. These electrical data demonstrate the capability to synthesize low-defect-density materials and form high-quality interfaces in N-face heterostructures.

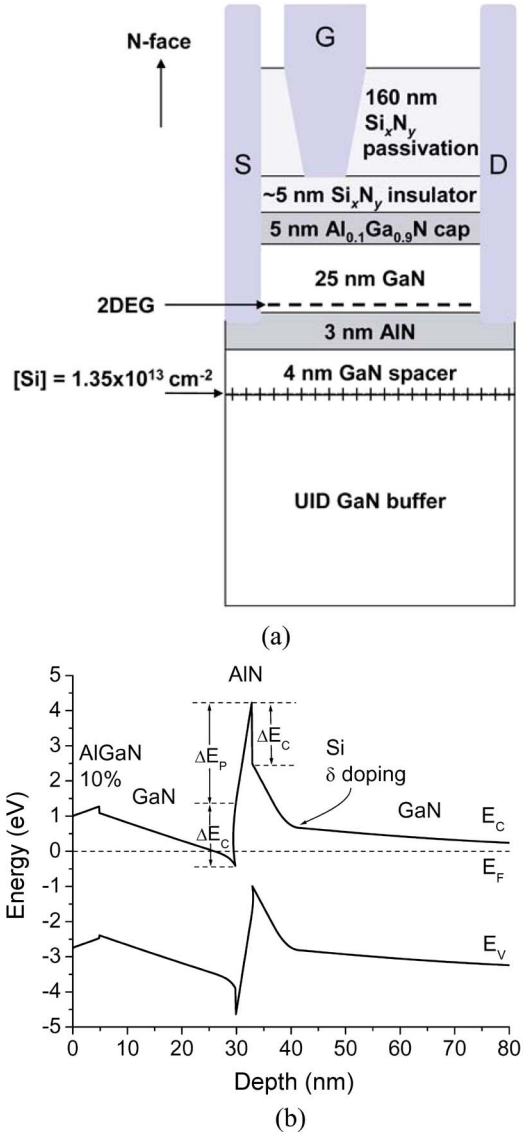

Fig. 1. (a) Schematic cross section and (b) simulated band diagram of the device.

In this letter, we present an N-face metal–insulator–semiconductor HEMT (MIS-HEMT) where a 2DEG is confined at a GaN (channel)/AlN (barrier) heterointerface by exploiting the benefits of using AlN to form the heterojunction [16]. Large-signal performance significantly improved from the results reported in [15] was achieved through optimized passivation technology and buffer growth, as will be further explained in the following section.

II. Device Design and Fabrication

The epitaxial structure and simulated band diagram (generated by a 1-D Schrödinger–Poisson solver [17]) of the HEMTs used in this letter are shown in Fig. 1. All devices were grown by nitrogen plasma-assisted molecular beam epitaxy on C-face 6H-SiC substrates at 710 °C. Initiating the growth with an N-rich AlN nucleation layer leads to low impurity incorporation from the substrate into the buffer and, hence, reliable insulating buffers [18]. A two-step GaN buffer of $\sim$0.5 μm thick was used, where the first 100 nm (step 1) reduced the threading dislocation density with rough growth, and the remaining thickness (step 2) recovered the surface morphology [13]. A silicon δ-doping of 1.35×10^{13} cm^{-2} was used to supply charges to the channel and prevent modulation of slow-responding trap states near the valence-band edge at the bottom AlN/GaN interface [19]. A 3-nm AlN barrier layer induced a 2DEG at the top GaN/AlN interface, above which a 25-nm GaN channel layer was grown. The electrons were further separated from the dopants by a 4-nm GaN spacer layer to reduce remote ionized impurity scattering. The devices were capped by 5 nm of $Al_{0.1}Ga_{0.9}N$, which prevented surface degradation during the subsequent deposition of a 5-nm-thick Si_xN_y gate insulator using high-temperature chemical vapor deposition (HTCVD) at 1020 °C in an MOCVD reactor. A thin cap layer with low Al content was chosen to minimize depletion of the 2DEG due to its reverse polarization field.

A schematic band diagram of the N-face HEMT is shown in Fig. 1. The large conduction-band discontinuity of GaN with AlN (ΔE_C), together with the large dipole moment (ΔE_P) of AlN strained to GaN due to the large polarization coefficients of AlN, enables the use of a thin layer of AlN for stronger back-barrier confinement than with an AlGaN alloy. For a 3-nm-thick AlN layer, Schrödinger–Poisson simulation (Fig. 1) estimated a 2DEG confinement potential to be larger than the bandgap energy of GaN. In addition, the use of a binary material for 2DEG confinement eliminates alloy scattering as a mechanism limiting low-field electron mobility.

The HEMT was fabricated by standard photolithography. A Ti/Al/Ni/Au (20/100/10/50 nm) multilayer stack, annealed at 870 °C for 30 s in N_2 atmosphere, was used for ohmic metallization. The HTCVD Si_xN_y and $Al_{0.1}Ga_{0.9}N$ in the contact areas were removed by dry etching prior to metal evaporation to facilitate ohmic contact formation. Mesas were formed with BCl_3/Cl_2 reactive ion etch. The surface was subsequently passivated with Si_xN_y by plasma-enhanced chemical vapor deposition (PECVD). A timed etch using CF_4/O_2 plasma was used to remove the PECVD Si_xN_y under the gate and to create a slanted sidewall profile [20] while keeping the HTCVD Si_xN_y as the gate insulator. Ni/Au/Ni (30/250/50 nm) was used as the gate metallization. Passivating the device prior to gate deposition ensured uniform Si_xN_y coverage at the edge of the gate metal. The devices were 2×75 μm wide with 0.7-μm nominal gate length and 0.5-μm gate–source spacing. The source–drain spacing was 2.2 μm.

III. Results and Discussion

Hall measurements were taken at room temperature using the Van der Pauw geometry. The 2DEG density and mobility were 7.7×10^{12} cm^{-2} and 1350 cm^2/V $\cdot$ s, respectively. The contact resistance, measured using the four-point probe transfer length method, was 0.8 $\Omega \cdot$ mm. The maximum drain current $I_{\max}$ was 0.8 A/mm at $V_G = +2$ V (Fig. 2). The buffer leakage at 1 mA/mm, measured between the source and drain of a transistor with the channel being etched away, was in excess of 250 V. Two-terminal gate–drain breakdown voltage at 1 mA/mm was 48 V. The breakdown of the device might

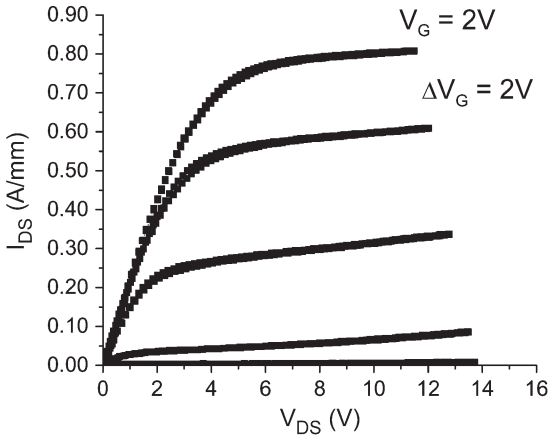

Fig. 2. DC I–V of the device.

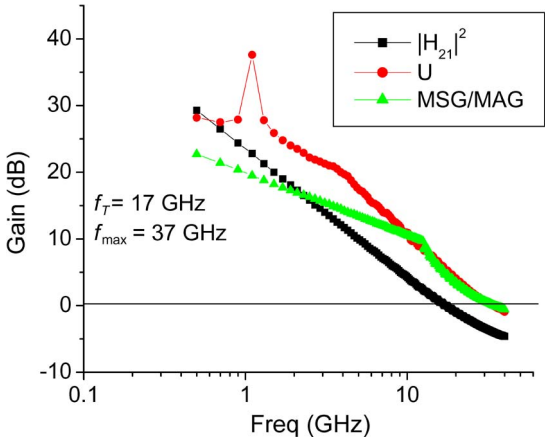

Fig. 3. Small-signal performance of the device.

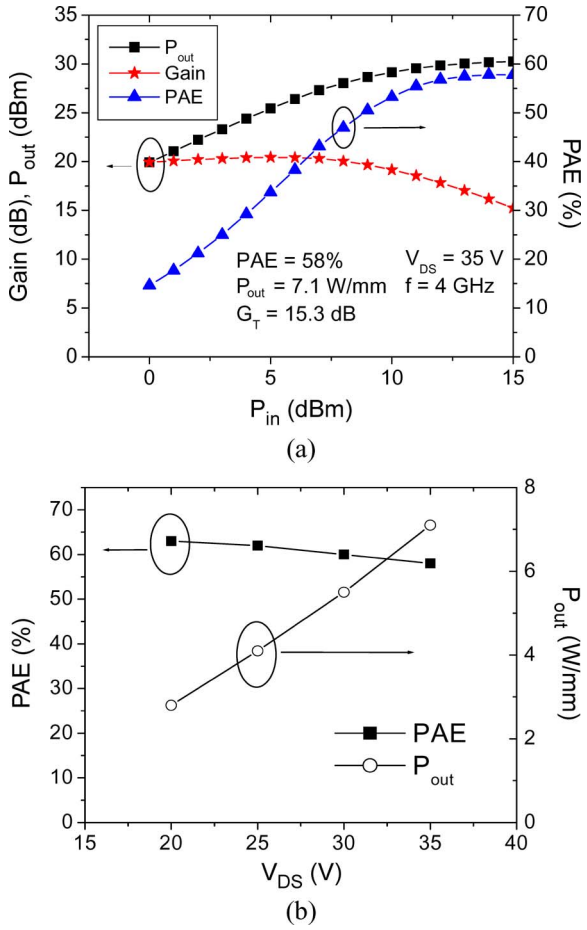

Fig. 4. (a) Large-signal performance of the device at 4 GHz. (b) Dependence of microwave output power density and PAE on drain bias.

have been impacted by the high electric field sustained in the GaN channel layer when the gate–drain diode was reverse biased, and could be improved by field-plate optimization or epitaxial design strategies proposed by Rajan *et al.* [14]. Gate-pulse measurements at 80 μs and 10% duty cycle, with the device being biased on a 50-Ω load line, did not indicate any dc–RF dispersion.

Small-signal high-frequency characterization was performed with an Agilent E8361A network analyzer. Linear extrapolation of the current gain and power gain, respectively, along a 20-dB/dec slope led to an f_T of 17 GHz and an $f_{\max}$ of 37 GHz at $I_{\rm DS} = 520$ mA/mm and $V_{\rm DS} = 25$ V (Fig. 3). Power measurements were performed using a Maury microwave load-pull system. Biased in deep class AB, measurements at 4 GHz with $V_{\rm DS} = 35$ V and a quiescent drain current density of 100 mA/mm yielded a transducer gain G_T of 15.3 dB and an output power density $P_{\rm out}$ of 7.1 W/mm with an associated power-added efficiency (PAE) of 58% (Fig. 4).

Load-pull measurements at 4 GHz for different drain biases were carried out, and the results are shown in Fig. 4. Only a slight drop in PAE is observed over the bias range. The high output power and its continued increase with drain bias indicate minimal dispersion in these devices. The optimal load impedance match for 35 V was found to have a resistive component of $\sim$600 Ω, which was the maximum value available. Higher efficiency is expected with increased charge density, which will lead to lower on-resistance, reduced knee voltage, higher drain current, and more optimal load impedance match at high drain biases without being limited by the maximum load reflection coefficient available from the load-pull system.

IV. Conclusion

In summary, an N-face MIS-HEMT with good dc and RF properties at the optical gate length was demonstrated. The use of AlN for electron confinement eliminates alloy scattering and offers a strong back-barrier to mitigate short-channel effects for highly scaled sub-micrometer devices. The results of this letter demonstrate that N-face devices can be used to generate microwave power, and represent an important step in engineering N-face devices toward delivering excellent power density and efficiency at microwave and millimeter-wave frequencies.

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