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Post-annealing effects on device performance of AlGaN/GaN HFETs

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Abstract

The effects of post-annealing on DC, RF, and power performances of AlGaN/GaN HEMTs with a gate-length of 0.3 μm were investigated. The results show that the post-annealing technique can improve the device breakdown voltage and device uniformity, reduce the trapping centers on AlGaN surface and/or GaN buffer layer after the post-annealing, and adjust the device threshold voltage. Specifically, after 20-min post-annealing at 400 °C, the gate-to-drain breakdown voltage of the device exhibits remarkable improvement from 10 to 187 V. The maximum extrinsic transconductance (g_m) increases from 238 to 254 mS/mm at a drain bias of 10 V after 10-min annealing at 400 °C. The threshold voltage shifts from −3.3 to −2.7 V. However, due to the decrease of two-dimensional electron gas concentration, the maximum drain current at a gate bias of 1 V reduces slightly from 918 to 904 mA/mm. The values of the unity current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}) increase after annealing. The output power and gain at 10 GHz were improved from 16.4 dBm and 11.4 dB to 22.4 dBm and 17.9 dB, respectively.

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Keywords: GaN; HEMT; Breakdown; Post-annealing

1. Introduction

GaN-based high electron mobility transistors (HEMTs) constitute the leading candidates for high temperature and high power microwave applications due to the unique material properties [1–4]. The wide bandgap of GaN and its alloys leads to high breakdown voltages for GaN-based HEMTs. A high breakdown voltage is crucial for power performances of microwave power devices and circuits, along with a high RF current, an efficient thermal management, and a low loss impedance matching circuit design. To improve breakdown voltage performance of GaN-based HEMTs, several attempts have been performed. A breakdown voltage of 570 V in an AlGaN/GaN HEMT with a source–drain spacing of 13 μm and a gate length of 0.5 μm using an overlapping gate structure has been reported [5]. Utilizing a gate dielectric layer, Fan et al. [6] reported AlGaN/GaN metal–oxide-semiconductor heterostructure field-effect transistors with a gate–drain breakdown voltage of 200 V for a SiO_2 1 μm-gate and a source–drain separation of 3 μm. However, for microwave power devices, the breakdown voltages are significantly lower, generally in the range of few tens of volts, mainly because of the small gate–drain spacing and small gate-length.

Recently, we investigated the thermal stability of Schottky contacts on strained AlGaN/GaN heterostructures. Under certain thermal stressing conditions, the reverse leakage current of Ni Schottky contacts on strain AlGaN/GaN heterostructures dramatically decreases more than three orders of magnitude lower than that of the reference sample without thermal stressing

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[7]. In this letter, we report the results of post-annealing effects on AlGaN/GaN HEMTs.

2. Device layer structure and fabrication

The epilayers of AlGaN/GaN HEMT structure were grown by metal-organic chemical vapor deposition (MOCVD) on a (0 0 0 1) sapphire substrate or a SiC substrate. The epilayer consists of 40 nm AlN nucleation layer, 3 μm of undoped GaN, and 20 nm undoped $Al_{0.3}Ga_{0.7}N$. Hall measurements indicated that the layer on sapphire substrate had a two-dimensional sheet carrier density of 1.2×10^{13} cm^{-2} and an electron mobility of 1175 $cm^2/V\,s$ at room temperature, respectively. Device isolation was performed by mesa dry etching using an inductively-coupled plasma reactive ion etching system in a chlorine-based plasma and using photoresist as an etch mask. Ti/Al/Mo/Au drain–source ohmic contacts were deposited using electron beam evaporation and annealed at 900 °C for sapphire substrate devices and 850 °C for SiC substrate devices for 30 s in a rapid thermal annealing system. The ohmic contact resistivity was determined typically to be 4×10^{-8} $\Omega\,cm^{-2}$ using transfer length measurement patterns; hence, excellent source access resistance was achieved. Ni/Au (60 nm/200 nm) metallization was used for Schottky gate contacts with a gate-length of 0.3 μm. The devices have a gate width of 100 μm and a source to drain spacing of 3 μm. The devices on sapphire substrate were chosen to optimize the post-annealing conditions. The sample on sapphire was cleft to few pieces and annealed for 5, 10, 20, 30, and 40 min at 270, 400, 600, and 700 °C in a furnace in N_2 ambient. After the post-annealing optimization, the sample with devices on SiC was annealed for 10 min at 400 °C. The measurements of DC, microwave, and power characteristics were performed using Agilent 4156C semiconductor parameter analyzer, Agilent 8510C network analyzer, and Focus tuner system.

3. Results and discussion

For the post-annealing optimization, the post-annealing for 10 min at 400 °C was determined as the optimum condition for maximum drain current and transconductance, while, for the breakdown voltage, 20-min annealing at 400 °C was the optimum. Fig. 1 shows the typical drain current–voltage characteristics of HEMT devices on SiC substrate with 0.3-μm gate-length and 100-μm gate-width before (solid lines) and after (dot lines) annealing at 400 °C for 10 min. The gate bias is in the range of −4 to 1 V with a step of 1 V. After 10-min annealing, the maximum drain current at a gate bias of 1 V has a slight drop from 918 to 904 mA/mm due to the decrease of two-dimensional electron gas concentration at the AlGaN and GaN interface. It was suggested that the diffusion of Ni atoms in the GaN layer affects the strain and surface states of the AlGaN which causes the decrease of polarization induced-charges [7]. After 20-min annealing, the maximum drain current at a gate bias of 1 V decreased to 788 mA/mm. Further increase of annealing time does not cause the measurable decrease of the maximum drain current. The contact resistance did not show distinguishable change for annealing conditions at lower than 600 °C for shorter than 30 min. However, for 700 °C after 20-min annealing, the ohmic contact resistance degrades from the range of 0.1–0.5 Ω mm to the range of 1.1–1.3 Ω mm. The device pinch-off voltage increases from −4 to −3 V after 10-min annealing due to a shorter effective gate-to-channel distance. However, as the annealing time increases further, the pinch-off voltage increases in magnitude. After 30-min annealing at 700 °C, the devices cannot be pinched off. We believe that it is because of the shunt path created by the diffusion of gate metal atoms. It should be pointed out that the post-annealing process improves trapping effects associated with the devices. The *I–V* characteristics of devices on sapphire substrate, before annealing, clearly show kinks at a drain bias of about 6 V, which have been attributed to the hot electron injection and the trapping in the buffer layer [8]. However, kinks practically disappeared after annealing. This suggests clearly that post-annealing may reduce the trapping centers in the GaN buffer layer.

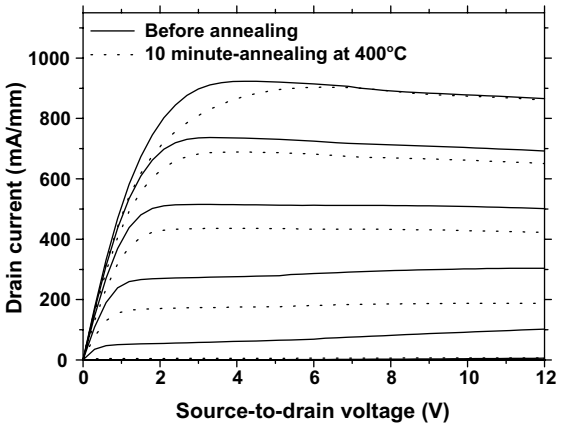

Fig. 1. *I–V* characteristics of the 0.3 μm AlGaN/GaN HEMT on SiC substrate before (solid line) and after 10-min annealing (dot line) in a furnace. The gate was biased from 1 to −4 V in a step of −1 V. After 10-min annealing at 400 °C, the maximum drain current at a gate bias of 1 V reduces slightly from 918 to 904 mA/mm.

Fig. 2 shows the typical transfer characteristics of device on SiC substrate before and after 10-min annealing at 400 °C. Before annealing, a maximum

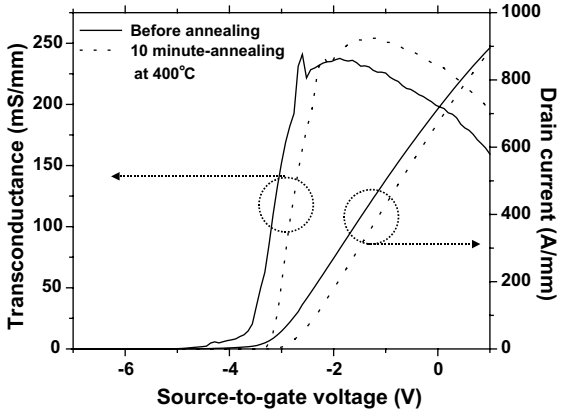

Fig. 2. Transfer characteristics of the 0.3 μm AlGaN/GaN HEMT on SiC substrate before (solid line) and after 10-min annealing at 400 °C (dot line) in a furnace. The drain bias was 10 V. Transconductance increases from 238 to 254 mS/mm due to increase of pinch-off voltage.

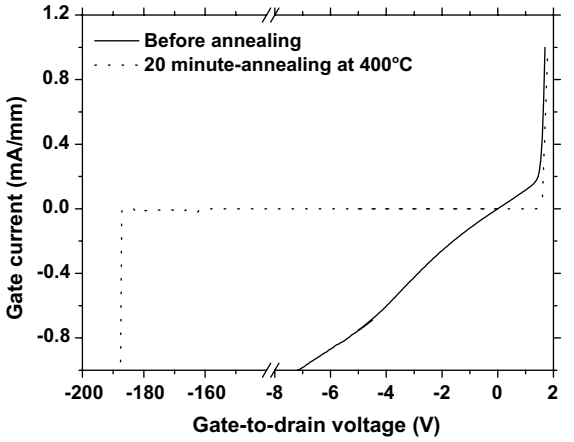

Fig. 3. Gate reverse current of the 0.3 μm AlGaN/GaN HEMT as a function of gate voltage before (solid line) and after 20-min annealing (dot line) at 400 °C. After annealing, the breakdown voltage improved from 7.5 to 187 V.

extrinsic transconductance (g_m) was measured 238 mS/mm at a gate voltage of −1.8 V and at a drain bias voltage of 10 V. It increases to 254 mS/mm at a gate voltage of −1.3 V at the same drain bias voltage after 10-min annealing at 400 °C, indicating a better gate modulation efficiency. From the gate bias intercept of the extrapolation of drain current curve at the peak g_m position in the transfer characteristics, the threshold voltages were determined. A threshold voltage of −3.3 V was measured for the device on SiC substrate before annealing. After 10-min annealing at 400 °C, the threshold voltage of the same device shifted to −2.7 V. However, after 20-min annealing at 400 °C, the transconductance decreases to 223 mS/mm because of the drain current degradation. The increase of threshold voltage is attributed to the reduction of effective thickness of AlGaN layer due to the diffusion of gate metal atoms, hence a shorter effective gate-to-channel distance. So, the post-annealing technique can be used to control the device threshold voltages by adjusting the annealing temperatures and duration time.

Fig. 3 shows reverse gate current characteristics of a device on sapphire substrate as a function of gate voltages before and after 20-min annealing at 400 °C. During measurements, the drain was shorted to the source. The gate-to-drain breakdown voltages were determined at a reverse gate leakage current of −1 mA/mm. The breakdown voltage before annealing is about 7.5 V. After 20-min post-annealing at 400 °C, the gate-to-drain breakdown voltage of the device on sapphire substrate increases to 187 V. This device exhibited reverse gate current of 2 μA at a gate bias of −30 V after 10-min annealing at 400 °C. The gate reverse current of the device on SiC substrate at gate bias of −30 V, which has breakdown voltage of 30 V before annealing, is 4 nA after 10-min annealing at 400 °C. This remarkable improvement on breakdown voltage performance is explained by the diffusion of Ni atoms affect the strain and surface states of the AlGaN layer, which causes the barrier height increase of Schottky contacts on strained AlGaN/GaN heterostructures. The improvement of breakdown voltage depends on annealing conditions. As the annealing time increases, at beginning, the breakdown voltage increases, however, after certain annealing time, it starts decreasing. For example, the breakdown voltage increases up to 20-min annealing time. After 30-min annealing, the breakdown voltage starts decreasing for devices annealed at 400 °C. Our recent pulsed measurements suggest that the traps with a short time constant play an important role on breakdown mechanisms.

The small signal RF measurements of AlGaN/GaN HEMTs were performed in the range of 1–35 GHz using an Agilent 8510C network analyzer. Fig. 4 shows the plots of the current gain $|H_{21}|$, the maximum stable power gain (MSG) and maximum available gain (MAG) versus frequency for the device on the sapphire after 30-min annealing at 400 °C. The values of the extrinsic unity current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}) increase from 23.1 and 61 GHz to 28 and 69 GHz, respectively. We noticed that the values of f_T and f_{MAX} varied with devices crossing the sample before post-annealing was performed. After annealing, the f_T and f_{MAX} values of devices are very uniform, indicating much better device uniformity.

Microwave power performance of the device on SiC substrate was measured at 10 GHz. Fig. 5 shows the typical power characteristics of the devices on SiC

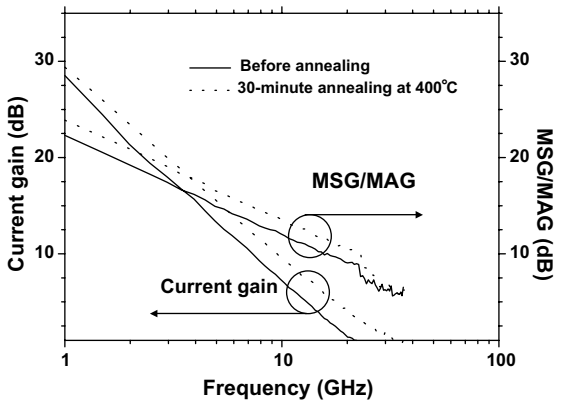

Fig. 4. Current gain and maximum stable power gain (MSG)/maximum available power gain (MAG) versus frequency of the 0.3 μm AlGaN/GaN HEMT before (solid line) and after annealing (dot line) at 400 °C for 30 min. Biasing conditions: before annealing, $V_G = -2.5$ V, $V_D = 10$ V; after annealing, $V_G = -3$ V, $V_D = 10$ V.

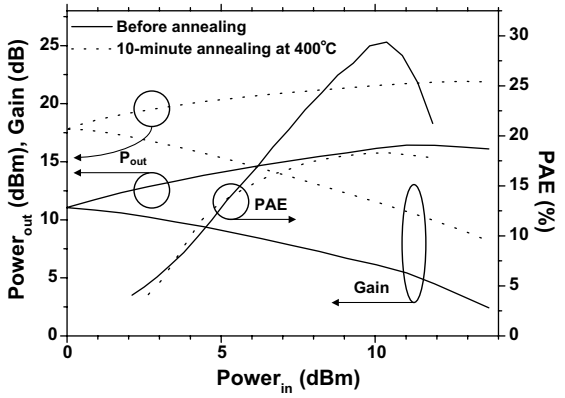

Fig. 5. Microwave power characteristics of the 0.3 μm AlGaN/GaN HEMT at 10 GHz before (solid line) and after 10-min annealing at 400 °C dot line. Biasing conditions: before annealing, $V_G = -2.5$ V, $V_D = 8$ V; after annealing, $V_G = -2.9$ V, $V_D = 30$ V.

substrate before (a) and after 10-min annealing (b). Before annealing, output power of 16.4 dBm, gain of 11.5 dB, and power-added efficiency of 29.4% were obtained at a source-to-gate bias of −2.5 V, a source-to-drain bias of 8 V, and a drain current of 35 mA. After annealing, clear improvements on microwave power performance were observed. For the device annealed for 10 min at 400 °C, the device gives output power of 22.4 dBm, gain of 17.9 dB, and power-added efficiency of 18.5% were obtained at source-to-gate bias of −2.9 V, source-to-drain bias of 30 V, and drain current of 22 mA. The improvement on power performance is attributed to the improved breakdown performance. So the devices after post-annealing can be biased at higher voltages.

4. Conclusion

The effects of post-annealing on DC, RF, and microwave power characteristics of AlGaN/GaN HEMTs with a gate length of 0.3 μm and a gate width of 100 μm were investigated. After 20-min annealing at 400 °C, the breakdown voltages of the devices on sapphire substrate were enhanced remarkably from 7.5 to 187 V. The threshold voltage shifted from −3.3 to −2.7 V. The kinks in device I–V characteristics disappeared, which is attributed to the removal of traps in the GaN buffer during annealing. After post-annealing, the devices exhibited also better uniformity.

These results demonstrated that a remarkable increase on breakdown voltages, improvement on gain and output power, reduction of traps on AlGaN surface and/or in the GaN buffer, improvement of device uniformity, and adjustment of threshold voltages for GaN-based HEMT after the post-processing annealing process.

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