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Postprocessing annealing effects on direct current and microwave performance of AlGaN/GaN high electron mobility transistors

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The effects of postprocessing annealing on direct current, radio frequency small signal, and power performances of AlGaN/GaN high electron mobility transistors with a gate-length of 0.2 μm were investigated. The postannealing technique can improve the device performance, especially, after 10 min postannealing at 400 °C, the gate-to-drain breakdown voltage of devices exhibits remarkable improvement from 25 to 187 V. The maximum extrinsic transconductance increases from 223 to 233 mS/mm at a drain bias of 10 V after 10 min annealing at 400 °C. The maximum drain current at a gate bias of 1 V increases from 823 to 956 mA/mm. After annealing, the values of the unity current gain cut-off frequency and the maximum oscillation frequency increases from 24 and 80 GHz to 55 and 150 GHz, respectively. The output power and gain at 10 GHz were improved from 16.4 dBm and 11.4 dB to 25.9 dBm and 19 dB, respectively. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1797556]

GaN-based high electron mobility transistors (HEMTs) are promising candidates for high temperature and high power microwave applications due to the material properties such as large band gap energy, high saturation velocity, and high drain current density.[1–4] The wide band gap of GaN-related materials leads to high breakdown voltages for GaN-based HEMTs. Devices with higher breakdown voltage are always required for extremely high microwave or millimeter wave power applications. Several attempts to improve breakdown voltage performance of GaN-based HEMTs have been performed, including using a field plate.[5] Recently, we investigated the thermal stability of Schottky contacts on strained AlGaN/GaN heterostructures. Under certain thermal stressing conditions, the reverse leakage current of Ni Schottky contacts on strained AlGaN/GaN heterostructures dramatically decreases more than three orders of magnitude lower than that of the control sample with no thermal stressing.[6] This letter reports that the postannealing technique could be a simple method to improve device performances of AlGaN/GaN HEMTs, especially breakdown voltage and microwave power performance.

The epilayers of AlGaN/GaN HEMT structure were grown by metalorganic chemical vapor deposition on a SiC substrate and on a sapphire substrate with an identical layer structure. The epilayer consists of 40 nm AlN nucleation layer, 3 μm of undoped GaN, and 20 nm undoped $Al_{0.3}Ga_{0.7}N$. Device isolation was performed by mesa dry etching using an inductively coupled plasma reactive ion etching system in a chlorine-based plasma and using photoresist as an etching mask. Ti/Al/Mo/Au drain-source ohmic contacts were deposited using electron beam evaporation and annealed at 850 °C for devices on SiC substrate for 30 s in a rapid thermal annealing system. Ni/Au(60 nm/200 nm) metallization was used for Schottky gate contacts with a gate length of 0.2 μm. The devices have a gate width of 100 μm and a source to drain spacing of 3 μm. For process optimization, the sample on sapphire was cleft to few pieces and annealed for 5, 10, 20, 30, and 40 min at 270, 400, 600, 700 °C in a furnace in N_2 ambient. After the postannealing optimization, the sample with devices on SiC was annealed for 10 min at 400 °C. The measurements of dc, pulsed-IV, microwave, and power characteristics were performed using Agilent 4156C semiconductor parameter analyzer, Dynamic IV analyzer (DINA), Agilent 8510C network analyzer, and Focus load-pull system.

Figure 1 shows the typical drain current-voltage characteristics of AlGaN/GaN HEMTs on SiC substrate with 0.2 μm gate-length and 100 μm gate-width before (solid lines) and after (dot lines) annealing at 400 °C for 10 min. The gate bias is in the range of −4 to 1 V with a step of 1 V. After 10 min annealing, the maximum drain current at a gate bias of 1 V increases from 823 to 956 mA/mm. The contact resistance did not show distinguishable change for annealing conditions at lower than 600 °C and for shorter than 30 min. As shown in Fig. 1, after 10 min annealing at 400 °C, the devices can still be pinched off at $V_g = -4$ V even with larger drain current drive capability. This may be attributed to a

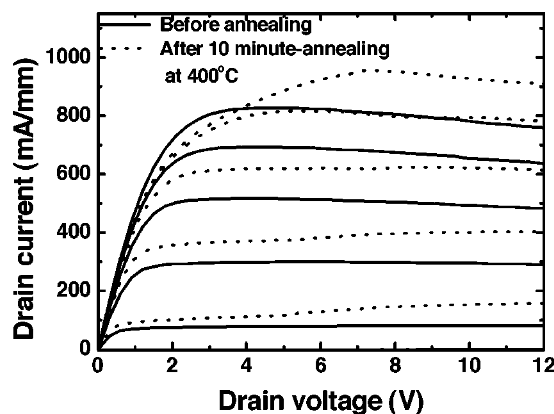

FIG. 1. $I-V$ characteristics of the 0.2 μm AlGaN/GaN HEMTs on SiC substrate before (solid lines) and after 10 min annealing (dashed lines) in a furnace. The gate was biased from −4 to 1 V in a step of 1 V. After 10 min annealing at 400 °C, the maximum drain current at a gate bias of 1 V increases from 823 to 956 mA/mm.

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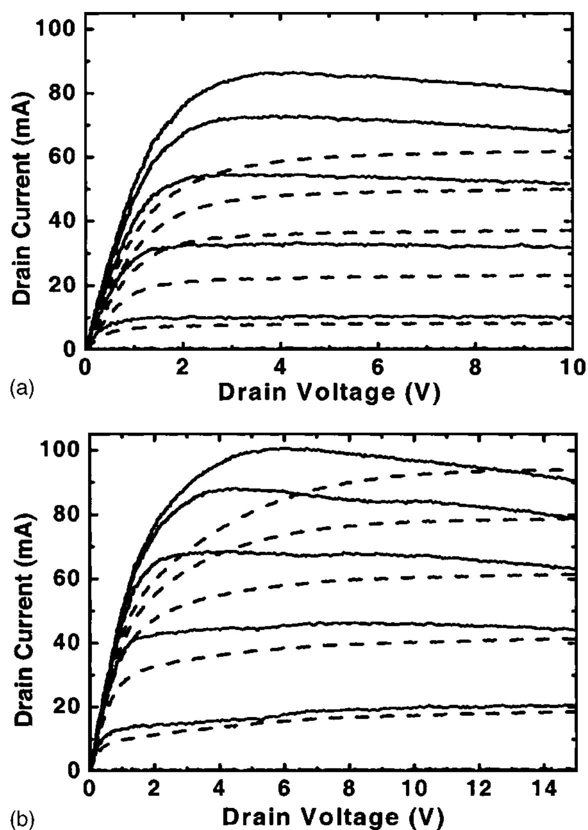

FIG. 2. Pulsed $I-V$ characteristics of unannealed (solid lines) and 10 min annealed AlGaN/GaN HEMTs at 400 °C, with dc $I-V$ characteristics for comparison. Quievscent bias point of (V_{DS0}, V_{GS0}) is (7 V, –5 V). The pulse duration is 2 μs with a period of 1 ms.

smaller effective gate-to-channel distance due to vertical diffusion of gate metal, and hence a better gate modulation efficiency. However, as the annealing time and temperature increase further, the pinch-off voltage increases in magnitude. After 40 min annealing at 700°C, the devices cannot be pinched off. We believe that it is because of the shunt path created by the diffusion of gate metal atoms.[6]

Figure 2(a) and 2(b) shows the typical pulsed $I-V$ characteristics (dashed lines) of umannealed and 10 min annealed devices, respectively, with $I-V$ characteristics under dc bias condition (solid lines) for comparison. Quiescent bias point of (V_{DS0}, V_{GS0}) is (7 V, –5 V). The pulse duration is 2 μs with a period of 1 ms. Unannealed devices show larger current dispersion than the 10 min devices, which demonstrates that the unannealed devices exhibit more trapping effects. Therefore, the increase of dc in annealed sample could be attributed to the increase of the two-dimensional electron gas concentration due to the reduction of trapping effect on AlGaN surface and/or GaN buffer layer after the postannealing.

Figure 3 shows the typical transfer characteristics of devices on SiC substrate before and after 10 min annealing at 400 °C. Before annealing, a maximum extrinsic transconductance (g_m) of 223 mS/mm was measured at a gate voltage of –2.2 V and at a drain bias voltage of 10 V. It increases to 233 mS/mm at a gate voltage of –2.1 V at the same drain bias voltage after 10 min annealing at 400 °C, indicating a better gate modulation efficiency. From the gate-bias intercept of the extrapolation of drain current curve at the peak g_m position in the transfer characteristics, the

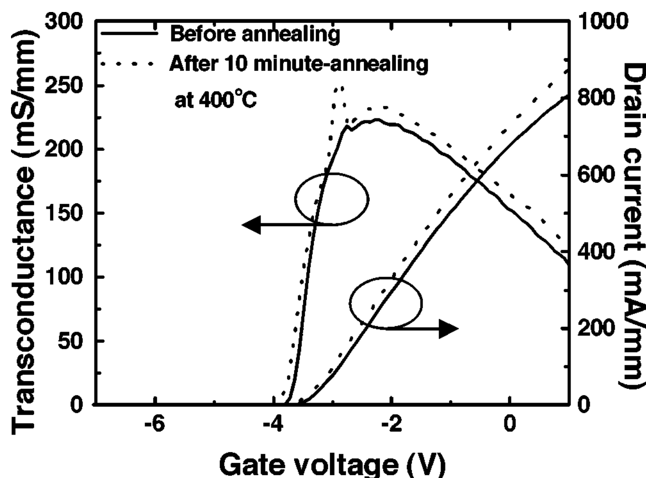

FIG. 3. Transfer characteristics of the 0.2 μm AlGaN/GaN HEMT on SiC substrate before (solid lines) and after 10 min annealing at 400 °C (dashed lines) in a furnace. The peak extrinsic transconductance increases from 223 to 233 mS/mm due to increase of pinch-off voltage. The drain bias is 10 V.

threshold voltages were determined. A threshold voltage of –3.3 V was measured for the device on SiC substrate before annealing. After 10 min annealing at 400 °C, the threshold voltage of the same device shifted to –3.6 V. It is suggested that post processing annealing reduces the trapping effects and decreases the filling of the interface levels, hence the source-drain current drive capability is improved. The decrease of trapping effects causes an increasingly negative shift in the threshold voltage. So, the postprocessing annealing technique can be used to control the device threshold voltages by adjusting the annealing temperatures and duration time.

Figure 4 shows reverse gate current characteristics of a device as a function of gate voltages before and after 10 minannealing at 400 °C. During measurements, the drain was shorted to the source. The gate-to-drain breakdown voltages were determined at a reverse gate leakage current of –1 mA/mm. The breakdown voltage before annealing is about 25 V. After 10 min postannealing at 400 °C, the gate-to-drain breakdown voltage of the device increases to 187 V. After annealing, it is observed that the dominant breakdown mechanism is physical, not electrical, due to the relatively thin gate metal thickness. The gate metals are broken at edge of mesa. Therefore, even higher breakdown voltages can be

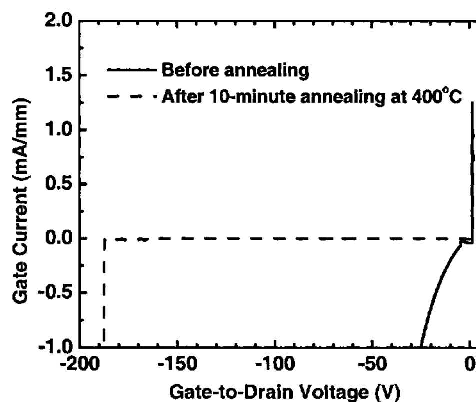

FIG. 4. Gate reverse current of the 0.2 μm AlGaN/GaN HEMT as a function of gate voltage before (solid line) and after 10 min annealing (dashed line) at 400 °C. The drain was shorted to the source. After annealing, the breakdown voltage improved from to 25 to 187 V.

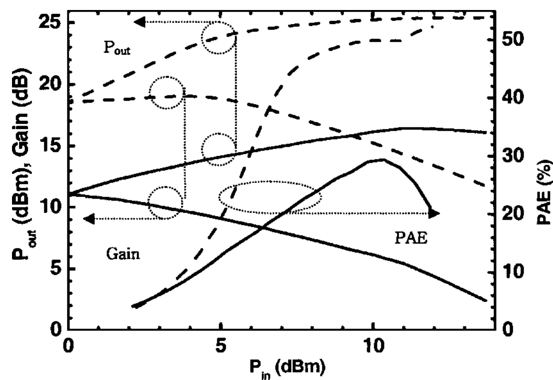

FIG. 5. Microwave power characteristics of the 0.2 μm AlGaN/GaN HEMT at 10 GHz before (solid lines) and after 10 min annealing at 400 °C (dashed lines). Biasing conditions: before annealing, $V_g=-2.5$ V, $V_d=8$ V; after annealing, $V_g=-2.7$ V, $V_d=30$ V.

expected with a thicker gate and overlay. This remarkable improvement on breakdown voltage performance is attributed to the fact that the vertical diffusion of Ni atoms affects the strain and surface states of the AlGaN layer, which causes the barrier height increase of Schottky contacts on strained AlGaN/GaN heterostructures. We observed that the breakdown voltage increases up to 20 min annealing time. After 30 min annealing, the breakdown voltage starts decreasing for devices annealed at 400 °C.

The small signal rf measurements of AlGaN/GaN HEMTs were performed in the range of 1–50 GHz using an Agilent 8510C network analyzer. After postannealing for 10 min at 400 °C, the values of the extrinsic unity current gain cut-off frequency (f_T) and the maximum oscillation frequency ($f_{\max}$) of the device on SiC substrate increase significantly from 24 and 80 GHz to 55 and 150 GHz, respectively. We noticed that the values of f_T and $f_{\max}$ varied with devices crossing the sample before postprocessing annealing. After annealing, the f_T and $f_{\max}$ values of devices are very uniform, indicating much better device uniformity.

Microwave power performance of the devices on SiC substrate before and after 10 min annealing at 400 °C was measured at 10 GHz. Figure 5 shows the typical power characteristics of the devices on SiC substrate before and after 10 min annealing at 400 °C. Before annealing, an output power (P_{out}) of 16.4 dBm, a gain of 11.5 dB, and a power-added efficiency (PAE) of 29.4% were obtained at a gate bias of −2.5 V, a drain bias of 8 V, and a drain current of 35 mA. For the device annealed for 10 min at 400 °C, a p_{out} of 25.9 dBm, a gain of 19 dB, and PAE of 52.5% were obtained at a gate bias of −2.7 V, a drain bias of 30 V, and the drain current of 22 mA. This is attributed to the improved breakdown performance. So the devices after post processing-annealing can be biased at much higher voltages to achieve higher output power and efficiency.

In summary, this letter demonstrates that the breakdown performance of AlGaN/GaN HEMTs can be improved by a simple postprocessing annealing process after Schottky gate metallization. The effects of postannealing on dc, rf, and microwave power characteristics of AlGaN/GaN HEMTs with a gate length of 0.2 μm and a gate width of 100 μm have been investigated. Using an optimized process, the drain current drive capability, extrinsic g_m, f_T, and $f_{\max}$, P_{out}, and PAE can be improved as well as the breakdown performance. Especially, after postanneling at 400 for 10 min, the maximum drain current at a gate bias of 1 V increases from 823 to 956 mA/mm. The transconductance of the devices was improved from 223 to 233 mS/mm. The breakdown voltages of the devices were enhanced remarkably from 25 to 187 V. The threshold voltage exhibited a negative shift. The values f_T and $f_{\max}$ increases from 24 and 80 GHz to 55 and 150 GHz, respectively. The output power and gain at 10 GHz were improved from 16.4 dBm and 11.4 dB to 25.9 dBm and 19 dB, respectively. The PAE is improved from 29.4% to 52.5%. After postprocessing annealing, the devices exhibited also better uniformity.

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[1]Y. F. Wu, D. Kapolnek, J. Ibbetson, N. Q. Zhang, P. Parikh, B. P. Keller, and U. K. Mishra, Tech. Dig. - Int. Electron Devices Meet. **1999**, 927.
[2]S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, and J. W. Palmour, IEEE Electron Device Lett. **20**, 161 (1999).
[3]N. X. Nguyen, M. Micovic, W. S. Wong, P. Hashimoto, L. M. McCray, P. Janke, and C. Nguyen, Electron. Lett. **36**, 468 (2000).
[4]V. Kumar, W. Lu, F. A. Khan, R. Schwindt, E. Piner, and I. Adesida, Electron. Lett. **37**, 1483 (2001).
[5]N. Q. Zhang, S. Keller, G. Parish, S. Heikman, S. P. DenBaars, and U. K. Mishra, IEEE Electron Device Lett. **33**, 1413 (2000).
[6]Z. Lin, H. Kim, J. Lee, and W. Lu, Appl. Phys. Lett. **84**, 1585 (2004).

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