achieved by the time variable transformation can be equivalently expressed by writing $k(\theta) = k(x, y, z, t)$, giving

$$\nabla_{tt}^2\theta + \frac{g}{\kappa_S} = \frac{1}{k(x,y,z,t)}\frac{\partial\theta}{\partial t} \qquad (3)$$

This equation is now fully linear, but $k(x, y, z, t)$ is not known *a priori* and must be obtained self-consistently, as described in [3]. The time variable transformation then corresponds essentially to the replacement, $k_S\Delta t \to k_S\Delta\tau = k_i\Delta t$, in the numerical solution of the nonlinear problem. k_i equals $k(x, y, z, t)$ at spatial node i and at a given time step.

Such a solution can be implemented within the authors' fully analytical thermal resistance matrix approach. Writing

$$\nabla^2\theta + \frac{g}{\kappa_S} = \sum_j f_j(x,y,z)\alpha_j(t) \qquad (4)$$

$$\frac{1}{k(\theta)}\frac{\partial\theta}{\partial t} = \sum_j f_j(x,y,z)\alpha_j(t) \qquad (5)$$

where the f_j are specified and the α_j are to be determined, eqn. 4 can be solved analytically in rectangular subvolumes, as described by the authors in [5]. Evaluating this analytical solution at points, (x_i, y_i, z_i), temperature rises above some boundary condition defined constants are calculated as

$$\Delta\theta_i(t) = \sum_j R_{ij}\alpha_j(t) \qquad (6)$$

The time-independent matrix, **R**, is not the thermal resistance matrix in the conventional sense, but is constructed using the same accelerated series methods [6]. **R** for complex structures is readily obtained by combining rectangular subvolume solutions [5].

Substituting for the $\alpha_j(t)$ from eqn. 6, in eqn. 5, a system of coupled first order ordinary differential equations for the $\Delta\theta_i(t)$ is obtained. Choosing the simplest explicit, numerical, time domain solution scheme for illustration, the recursive algebraic relation

$$\Delta\theta_i^{(n+1)} = \sum_j M_{ij}^{(n)}\Delta\theta_j^{(n)} \qquad (7)$$

is obtained at timestep $n + 1$, where system matrix $M_{ij}^{(n)} = \delta_{ij} + \Sigma_k\Delta t k_i^{(n)} f_{ik} R_{kj}^{-1}$ and $f_{ik} = f_k(x_i, y_i, z_i)$. With proper choice of the f_j and placement of the α_j, the number of nodes required in this dense matrix formulation, $j = 1, ..., N$, need be no more than that of a conventional boundary element method [3].

This approach is shown for the example presented by Krabbenhoft and Damkilde in [1]. Using, $f_j(x) = |x - x_j|$, and imposing the boundary conditions, $\theta(x = 0, t) = \theta_0$ and $\theta(x = L, t) = 0$, the result of Fig. 1 is obtained. Curve (ii), solid line, shows the fully analytical Fujita solution for $\lambda = 0.965$; curve (ii), dashed line, shows the result of the extended transformation approach. Agreement is essentially exact at all but the smallest times.

Conclusion: The time variable transformation described in [2], for solution of the nonlinear diffusion problem, is demonstrated to provide an alternative approximation to use of a mean diffusivity, for moderate nonlinearities such as those occurring in semiconductor systems. Importantly, this approach is compatible with compact thermal model construction, for rapid, coupled electro-thermal CAD. It avoids the need for computationally intensive numerical thermal solutions which are totally impractical in the necessarily iterative treatment of large, coupled electrical-thermal problems.

For an arbitrary temperature dependence of material parameters, the method described in [2] can be further developed within the authors' fully analytical thermal resistance matrix framework providing an alternative to conventional numerical approaches, such as finite difference, finite element or boundary element methods. However, this solution is not as economical as the original approximation. The problem of the minimal compact description of strongly temperature dependent diffusivity therefore still requires solution. Further development of a time variable transformation approach may yet prove useful in this context.

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Recessed 0.25 μm gate AlGaN/GaN HEMTs on SiC with high gate-drain breakdown voltage using ICP-RIE

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Using inductively coupled plasma reactive ion etching (ICP-RIE), recessed 0.25 μm gate-length AlGaN/GaN high electron mobility transistors (HEMTs) have been fabricated. A post-etch anneal eliminated the plasma-induced damage resulting in an improvement of the gate-drain breakdown voltage from –27 V for the as-etched to over –90 V for the annealed devices. The gate leakage current reduced from 91 to 4 μA at V_{gd} = –25 V, after annealing. These devices exhibited maximum drain current density of 770 mA/mm, unity gain cutoff frequency (f_T) of 48 GHz, and maximum frequency of oscillation (f_{max}) of 108 GHz.

GaN-based high electron mobility transistors (HEMTs) are promising devices for high power and high temperature applications [1 – 3]. This potential is due to the advantageous material properties such as wide bandgap leading to high breakdown voltage, high saturated-electron drift velocity and the existence of AlGaN/GaN heterostructure with high conduction band offset and high piezoelectricity resulting in high sheet carrier densities in the 10^{13} cm^{-2} range. Recently, tremendous progress has been recorded in the material quality and device processing of GaN-based HEMTs. These have resulted in significant improvements in the DC and RF performances of these devices [4]. Further improvements in device performance are expected by using recessed-gate structures. However, to date, there are only a few reports on recessed-gate structure AlGaN/GaN HEMTs using dry etching methods [5, 6]. The inertness of GaN materials dictates the use of dry etching techniques involving energetic particles. Bombardment with energetic ions can yield unsatisfactory results. Exposure of the gate area of FETs to plasma causes ion-induced damage resulting in the increase of gate leakage current and reduction of breakdown voltage, which are undesirable for high power and high temperature application. The use of low energy ions as found in ICP-RIE and a post-etch anneal can ameliorate these deleterious effects, and this has not been properly addressed to date.

In this Letter, for the first time, we present the DC and RF performance of recessed-gate AlGaN/GaN HEMTs fabricated using

ICP-RIE. These 0.25 μm gate-length devices exhibited gate to drain breakdown over −90 V, leakage current as low as 4 μA at V_{GD} = −25 V, f_t of 48 GHz and f_{max} of 108 GHz. These results demonstrate significant improvements for recessed-gate AlGaN/GaN HEMTs.

The layer used in the present study was grown on silicon carbide substrates by metalorganic chemical vapour deposition (MOCVD). The epilayer consists of 2 μm undoped GaN, 3 nm undoped $Al_{0.25}Ga_{0.75}N$ spacer, 10 nm $Al_{0.25}Ga_{0.75}N$ with a doping level of 6×10^{18} cm^{-3}, 10 nm undoped $Al_{0.25}Ga_{0.75}N$ and 40 nm thick Si-doped (9×10^{18} cm^{-3}) *n*-GaN cap layer. Hall measurements gave a sheet carrier concentration of 1.35×10^{13} cm^{-2} and an electron mobility of 757 cm^2/Vs. Device fabrication started with mesa isolation using Cl_2 plasma in an inductively coupled plasma reactive ion etch (ICP-RIE) system. Ohmic contacts were formed by rapid thermal annealing of evaporated Ti/Al/Ti/Au at 860°C for 30 s. Using on-wafer transfer length measurement (TLM) patterns, the ohmic contact resistance was typically measured to be ~0.30 Ωmm. Silicon nitride was deposited by PECVD as an etch mask for gate recessing. Then, electron beam lithography followed by ICP-RIE in SF_6 was used to pattern 1 μm recess windows centred between source and drain. Gate recessing was performed using ICP-RIE in Cl_2/Ar plasma at 3 mT and −50 V bias. After recess, one set of sample was rapid thermally annealed at 750°C for 1 min to eliminate plasma-induced damage [7]. Mushroom-shaped gates (Ni/Au) with gate-length (L_g) of 0.25 μm were fabricated using electron-beam lithography. The devices had a gate width of 100 μm and a source drain spacing of 3 μm.

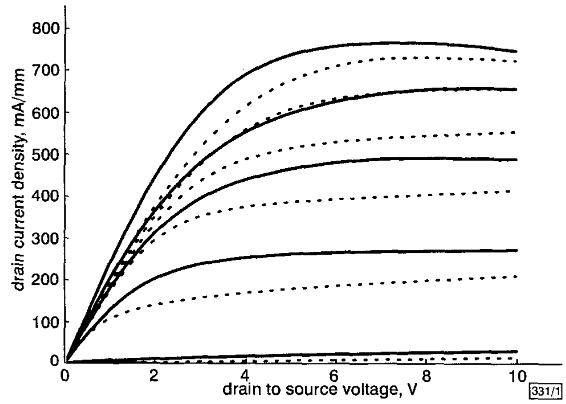

Fig. 1 *DC I_D-V_{DS} characteristics of recessed 0.25 μm × 100 μm AlGaN/GaN HEMTs on SiC substrates*

Gate bias was swept from 2 to −8 V in steps of −2 V
– – – – as-etched
——— post-etch annealed

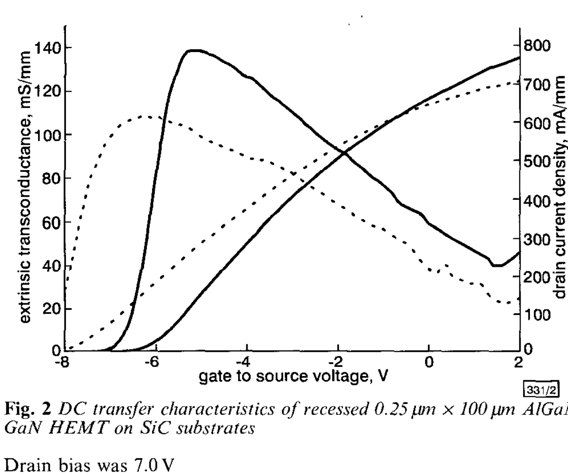

Fig. 2 *DC transfer characteristics of recessed 0.25 μm × 100 μm AlGaN/GaN HEMT on SiC substrates*

Drain bias was 7.0 V
– – – – as-etched
——— post-etch annealed

Measurements were conducted on both as-etched and post-etch annealed devices using an HP4145B semiconductor parameter analyser. Shown in Fig. 1 are the typical drain current-voltage (I_D-V_{DS}) characteristics of the devices. The gate was biased from 2 to −8 V in steps of −2 V. The as-etched devices exhibited a maximum drain current density of 730 mA/mm while a slightly higher current density of 770 mA/mm was measured on post-etch annealed devices. Also, pinch-off voltage is lower for the annealed devices. The DC transfer characteristics are shown in Fig. 2. The drain was biased at 7 V. A peak extrinsic transconductance (g_m) of 139 mS/mm was measured for the post-etch annealed devices while as-etched devices produced a peak g_m of 109 mS/mm. The effect of post-etch anneal on the gate to drain I-V characteristics is shown in Fig. 3. The gate-to-drain breakdown voltage increased from −27 V to over −90 V after post-etch anneal. Also, gate leakage current was significantly reduced and is as low as 4 μA at V_{gd} = −25 V. These improvements in device performance are attributed to the recovery of plasma damage by annealing. To the best of the authors' knowledge, this is highest ever reported value of gate-drain breakdown voltage for recessed-gate GaN based HEMTs.

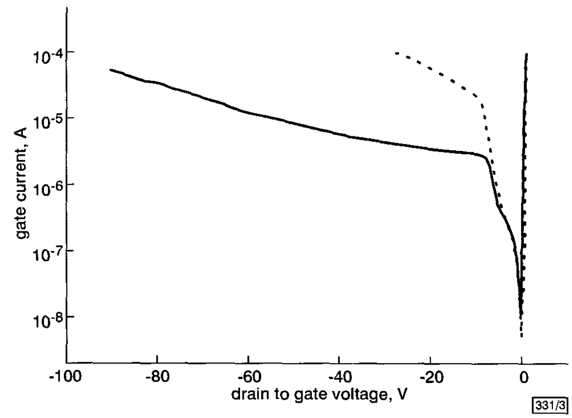

Fig. 3 *Gate to drain current-voltage characterstics of recessed 0.25 μm × 100 μm AlGaN/GaN HEMT*

– – – – as-etched
——— post-etch annealed

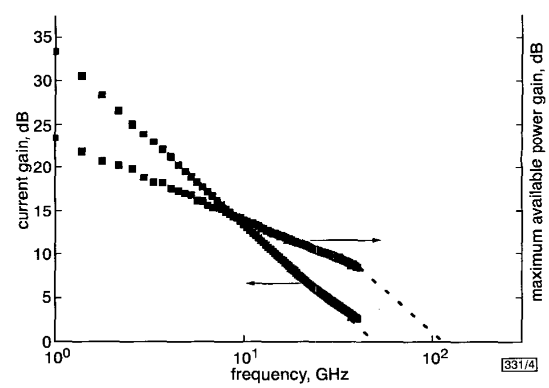

Fig. 4 *Short-circuit current gain ($|h_{21}|$) and maximum available power gain (G_{Amax}) of typical recessed 0.25 μm × 100 μm post-etch annealed AlGaN/GaN HEMT on SiC substrates*

Device was biased at V_{DS} = 10 V and V_{GS} = −5.45 V
f_T = 48 GHz, f_{max} = 108 GHz

RF measurements were carried out on-wafer using an HP8510B network analyser in the 1–40 GHz range. Fig. 4 shows the short-circuit current gain ($|h_{21}|$) and maximum available power gain (G_{Amax}) derived from on wafer S-parameters measurements against frequency on post-etch annealed devices. The values of unity gain cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) were determined by extrapolation of the $|h_{21}|$ and G_{Amax} data at −20 dB/decade. At a drain bias of 10 V and a gate bias of −5.45 V, an f_T of 48 GHz and f_{max} of 108 GHz were obtained, which are again the highest data ever reported for recessed-gate AlGaN/GaN-HEMTs.

In summary, we have presented the fabrication of recessed 0.25 μm gate-length AlGaN/GaN HEMTs using ICP-RIE. The post-etch anneal results in high gate-drain breakdown voltage and low gate leakage current. The measured values of gate-drain breakdown voltage of over –90 V, f_T of 48 GHz and f_{max} of 108 GHz are the highest ever reported data for recessed-gate AlGaN/GaN HEMTs.

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Threshold analysis in wavelet-based denoising

L. Zhang, P. Bao and Q. Pan

The hard threshold $t = c\sigma$ is efficient in wavelet threshold-based nonlinear filtering. In general, the optimal constant c would vary with the signal and the added noise. The nearly optimal choice of c by minimising $F(c)$, which is an equivalent function to the mean square error (MSE) of the recovered signal, is discussed. Experiment shows that $F(c)$ is consistent with the MSE.

Introduction: In wavelet-based signal denoising, an intuitive and efficient approach is to apply the preset threshold to the wavelet coefficients. Donoho [1] first gave a soft threshold $t = \sigma\sqrt{(2 \log M)}$, where σ is the standard deviation of noise and M is the length of signal. While this threshold possesses some minimax properties, it is non-intuitive and varies with M. Pan and Zhang [2] used a hard threshold $t = c\sigma$ to denoise signals effectively, where constant c is chosen as $c \in (3, 4)$ based on the fact that most of the noise values will fall within 3–4 times of its standard deviation.

For a given M or a fixed c, the two thresholds above will be invariant for all types of signals. In general, the optimal value of t or c would vary with the signals and noise. In this Letter, a function $F(c)$ that approximates an equivalent to the mean square error (MSE) of the recovered signal is constructed. The near optimal c can be determined by minimising $F(c)$.

Hard threshold-based denoising by wavelet transform: Suppose there is a sequence of observations $y_i = x_i + n_i$, $i = 1, 2, ..., M$, where $n_i \simeq N(0, \sigma^2)$ is white Gaussian noise. The goal is to estimate signal X from Y. Donoho [1] first developed a wavelet shrinkage method by a soft threshold $t = \sigma\sqrt{(2\log M)}$. Some impressive results were reported based on hard thresholding [2]. The procedure can be described as follows. First the sequence Y is transformed into wavelet coefficient W_Y; then hard threshold $t = c\sigma$ is applied on W_Y:

$$\hat{W}_Y(i) = \begin{cases} W_Y(i) & |W_Y(i)| \geq t \\ 0 & |W_Y(i)| < t \end{cases} \tag{1}$$

where $c \in (3, 4)$ is a constant; finally the estimation $\hat{Y}$ is reconstructed from $\hat{W}_Y$.

In general, for different signals and noise, the optimal c will be different. We now construct a function $F(c)$, nearly equivalent to the MSE of $\hat{Y}$, to determine c.

Determination of c: Orthogonal wavelet transform (OWT) is linear. Thus we have $W_Y = W_X + W_N$, where W_Y, W_X and W_N denote the OWT of observation Y, signal X and noise N, respectively. Similarly, we have $\hat{W}_Y = \hat{W}_X + \hat{W}_N$, where:

$$\begin{cases} \hat{W}_X(i) = W_X(i), \hat{W}_N(i) = W_N(i) & |W_Y(i)| \geq t \\ \hat{W}_X(i) = 0, \hat{W}_N(i) = 0 & |W_Y(i)| < t \end{cases} \tag{2}$$

We also have $\hat{Y} = \hat{X} + \hat{N}$, where $\hat{Y}$, $\hat{X}$ and $\hat{N}$ are the inverse OWT of $\hat{W}_Y$, $\hat{W}_X$ and $\hat{W}_N$.

Obviously, the optimal c, i.e. t, should minimise the MSE of $\hat{Y}$:

$$E[\tilde{Y}^2] = E[(\hat{Y} - X)^2] = min$$

Because $E[X^2]$ is independent of c, it is equivalent to minimising the following function:

$$Error(c) = E[\tilde{Y}^2] - E[X^2]$$

Since OWT is orthonormal, from eqn. 2 and $E[\hat{W}_X W_N] = 0$, we get:

$$Error(c) = 2E[\hat{W}_N^2] - E[\hat{W}_Y^2] \tag{3}$$

Suppose k points will be eliminated in $\hat{W}_Y$, we have:

$$E[\hat{W}_N^2] = \frac{1}{M}\sum_{i=1}^{M} W_N^2(i) - \frac{1}{M}\sum_{j=1}^{k} W_N'^2(j) \tag{4}$$

where $\hat{W}'_N$ denotes the k eliminated points in $\hat{W}_N$.

It is almost true that if $|W_Y(i)| < t$ then $|W_N(i)| < t$. This statement is validated by the tests on two typical signals in Fig. 1. Let $t = c\sigma$ and c increase from 1 to 4 with step-length 0.3. Denote K the number of points satisfying $|W_Y(i)| < t$ and K_N the number of points satisfying both $|W_Y(i)| < t$ and $|W_N(i)| < t$. The averaged results of K_N/K generated by the Monte Carlo experiment in signal-to-noise ratio (SNR) are listed in Table 1. In fact, when $t \geq \sigma$, for noise in any scale, K_N/K is nearly equal to 1, which implies that when $|W_Y(i)| < t$, $|W_N(i)| < t$ holds with high probability. The wavelets used in the experiments are Haar (for Blocks) and four taps orthogonal wavelet (for Bumps).

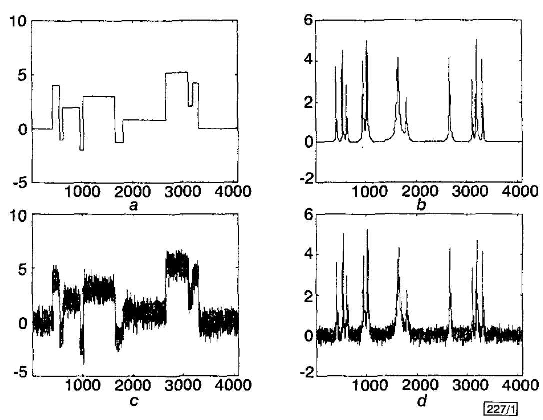

Fig. 1 *Two typical signals and their noisy versions*

a Blocks
b Bumps
c Noisy Blocks
d Noisy Bumps