Simulation of Short-Channel Effects in N- and Ga-Polar AlGaN/GaN HEMTs

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***Abstract*—We have carried out 2-D simulation of N-polar and Ga-polar AlGaN/GaN HEMTs to investigate short-channel effects in highly scaled devices. N-polar HEMTs were found to have better drain-induced barrier lowering (DIBL) suppression than Ga-polar HEMTs. The short-channel effects were found to originate from the 2-D potential distribution in the channel and space-charge-limited current through the buffer. The inverted structure of the N-polar HEMT was found to provide better suppression of short-channel effects under idealized theoretical assumptions that were used in the model presented.**

***Index Terms*—AlGaN/GaN high electron mobility transistor (HEMT), drain-induced barrier lowering (DIBL), Ga-polar, N-polar, short-channel effects, simulation, technology computer-aided design (TCAD).**

I. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have shown considerable improvements in performance in the last two decades. The inherent material properties such as high breakdown field, high mobility and saturated velocity, high thermal conductivity, and wide band gap make AlGaN/GaN HEMTs a promising candidate for many microwave power and low-noise applications. The combination of improved growth structures and fabrication techniques have enabled devices to obtain an outstanding output power performance of 40 W/mm at 4 GHz [1], a unity current gain cutoff frequency of 160 GHz [2], and a maximum frequency of oscillation of 300 GHz [3].

There have been considerable efforts to scale dimensions in III-nitride HEMTs to improve high-frequency performance of transistors. As in other material technologies, devices show short-channel effects as the gate length is reduced in HEMT devices, and the performance enhancement due to device scaling is restricted, even though the gate length can be shrunk down to 25 nm [4]. Various nonidealities are introduced due to device scaling, and efforts to mitigate these have included gate recessing to increase the device aspect ratio [5], the use of a double heterojunction structure [6], and an insulation of the buffer layer with p-type dopant [7]. Recently, inverted HEMT structures based on the N-polar ($\bar{c}$-axis) orientation of wurtzite GaN were investigated. These devices exploit the reversed direction of spontaneous and piezoelectric polarization and are expected to have several advantages over Ga-polar HEMTs, including better channel confinement, higher quantum capacitance [8], and improved ohmic contact resistance [9].

Even though several analytical models have been adopted into Ga-polar single-heterojunction HEMTs (Ga-SHEMTs) to analyze dc characteristics, there are few 2-D simulations of highly scaled devices [7], [10], [11]. In addition, there are no analytical or simulation models developed for Ga-polar double-heterojunction HEMTS (Ga-DHEMTs) and N-polar HEMTs (N-HEMTs). In this paper, we used 2-D device drift-diffusion-based simulation (Silvaco Atlas [18]) to investigate the operation of highly scaled III-nitride HEMTs grown in both Ga-polar and N-polar directions.

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II. Simulation

A. Device Structures

Simulations for the comparison of short-channel effects in three different AlGaN/GaN HEMT structures were carried out using the 2-D device simulator Silvaco ATLAS. To analyze and compare short-channel effects of both Ga- and N-HEMTs, we chose three different AlGaN/GaN HEMTs epitaxial structures. The first structure is a standard AlGaN/GaN HEMT with a cap composition of 30% and a thickness of 30 nm on top of 1 μm of GaN buffer layer [Ga-SHEMT, Fig. 1(a)]. AlGaN backbarriers were found to improve the short-channel performance in previous work [6]. We have therefore included a double-heterostructure HEMT consisting of 30 nm of 30% AlGaN cap layer on top of 30-nm GaN channel layer and 1 μm of 4% AlGaN backbarrier layer as the buffer layer to improve the charge confinement [Ga-DHEMT, Fig. 1(b)]. Finally, we simulated an N-polar HEMT consisting of 30-nm GaN channel layer on top, 30 nm of 30% AlGaN layer in the middle as a barrier layer, and 1-μm-thick GaN buffer layer on the bottom [N-HMET, Fig. 1(c)].

The gate–source and the gate–drain spacing were fixed at 0.1 and 0.5 μm, respectively. We have simulated 50-nm-gate-length devices for each epitaxial structure, and the cap layer is recessed under the gate by 20 nm, leading to a nominal-gate-to-channel distance of 10 nm. We used the metal work-function of Ni (5.2 eV) for the gate Schottky contact. The material parameters of $Al_xGa_{1-x}N$ semiconductor were also introduced into the simulation.

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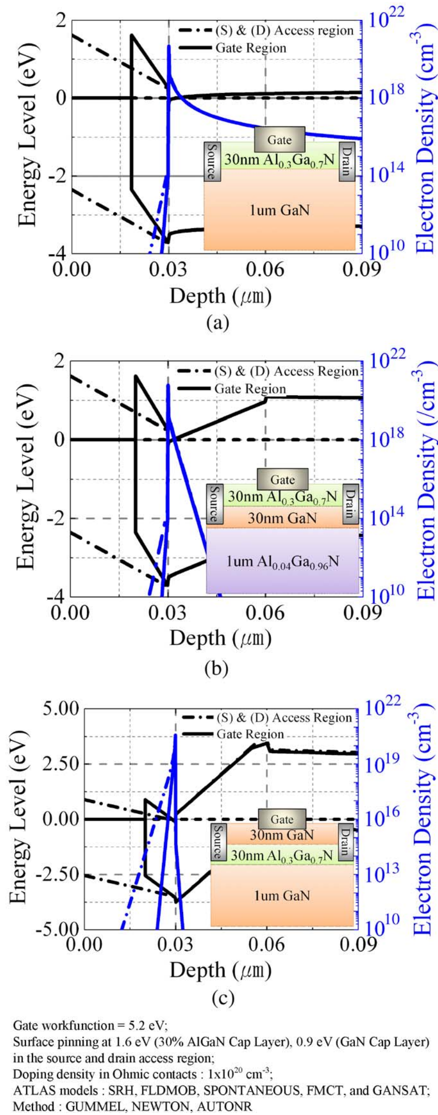

Fig. 1. Structure schematics and energy band diagrams. (a) Standard Ga-SHEMT. (b) Performance improved Ga-DHEMT. (c) Standard N-HEMT.

B. Physical Models

The composition-dependent material structure, spontaneous polarization, and piezoelectric polarization parameters were included in the simulation to introduce the correct polarization charges at the heterointerface [15]–[17]. Fig. 1(a)–(c) shows the calculated energy band diagrams (black) and charge distributions (blue) below the gate region (solid) and the access region (dashed-dot) in the growth (c-axis) direction. The charge densities of the 2-D electron gas (2-DEG) in the gate region (in the access region) for Ga-SHEMT, Ga-DHEMT, and N-HEMT were obtained as 1.11×10^{13} (1.45×10^{13}) cm^{-3}, 0.89×10^{13} (1.24×10^{13}) cm^{-3}, and 0.74×10^{13} (1.07×10^{13}) cm^{-3}, respectively. The pinchoff voltage (V_P) of each device with the recessed gate is obtained as -3, -2, and -2 V, respectively.

Palacios *et al.* [12] pointed out the discrepancy of the velocity-field relationship between Monte Carlo calculation and measured data. We used the experimentally measured velocity-field curves from [12] and applied the Farahmand Modified

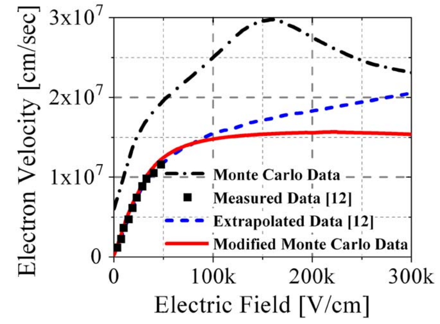

Fig. 2. Various electron velocity versus electric field profile. Monte Carlo data were obtained from Silvaco MOCASIM simulation.

Caughey–Thomas expression for group-III nitride material system [13], [14] in this paper. Fig. 2 depicts this new curve with Monte Carlo velocity-field curves and the extrapolated curve from [12]. Both N- and Ga-polar HEMT simulations used this curve for the electron transport.

In this paper, the effect of gate leakage current and charge quantization effects have not been taken into account. However, gate leakage current in an actual field-effect device can strongly affect the modulation and pinchoff characteristics. A thin AlGaN layer and a SiN insulator are added into an actual N-polar HEMT structure to minimize gate leakage current due to a low Schottky barrier height between gate metal and GaN in previous works [19], [20]. Introduction of high-k dielectric would be essential to mitigate the gate leakage in N-polar HEMTs while minimizing degradation due to short-channel effects.

III. Results and Discussions

DC current–voltage (I–V) characteristics of each HEMT are simulated for the gate biases (V_{GS}) from 0 V to $V_P - 1$ V, and for the drain biases from 0 to 10 V, which are depicted in Fig. 3(a)–(c). In Fig. 3, the solid line of each figure shows the I–V for their V_P. Short-channel effects are apparent not only from the large threshold voltage shifts but also from the high output conductance in both highly scaled Ga-polar HEMTs. However, N-HEMT maintains a low output conductance and minimizes the threshold voltage shift under the same scaling condition with two Ga-polar HEMTs. To show drain-induced barrier lowering (DIBL) more explicitly in a highly scaled device, we investigated the conduction band profiles. First, the 1-D conduction energy profiles in the channel of each device at pinchoff are shown in Fig. 4(a)–(c). The profiles were calculated at a gate bias of V_P [corresponding to the solid (blue) line in Fig. 3(a)–(c)] with the drain bias varied between 0 and 8 V.

Due to the poor aspect ratio, the gate channel control becomes worse, so that the drain bias affects the entire potential barrier in the channel of all three devices. The potential barrier between source and drain in both Ga-polar HEMTs is lowered as the drain bias increases. The poor channel control in Ga-polar HEMTs directly deteriorates the channel confinement and the output conductance. Moreover, for Ga-DHEMT [Fig. 4(b)], the potential barrier at its V_P is immediately lowered below the quasi-Fermi level as the drain bias starts to be

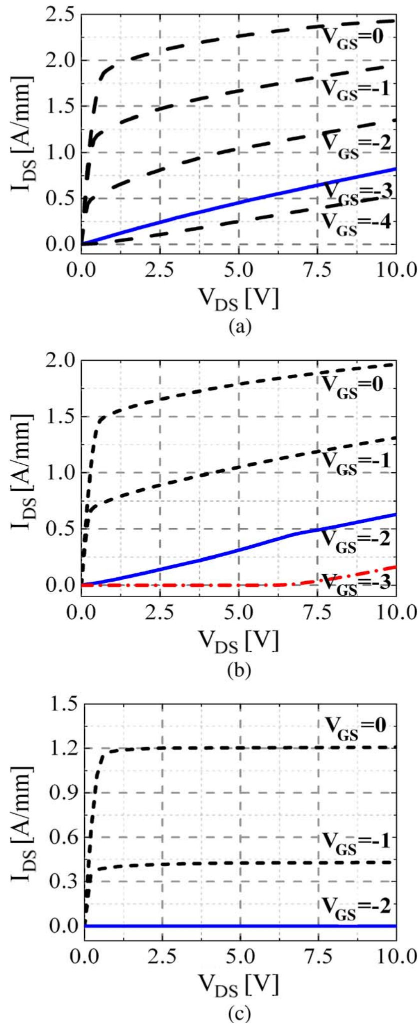

Fig. 3. Current–voltage characteristics of each device. (a) Ga-SHEMT. (b) Ga-DHEMT. (c) N-HEMT.

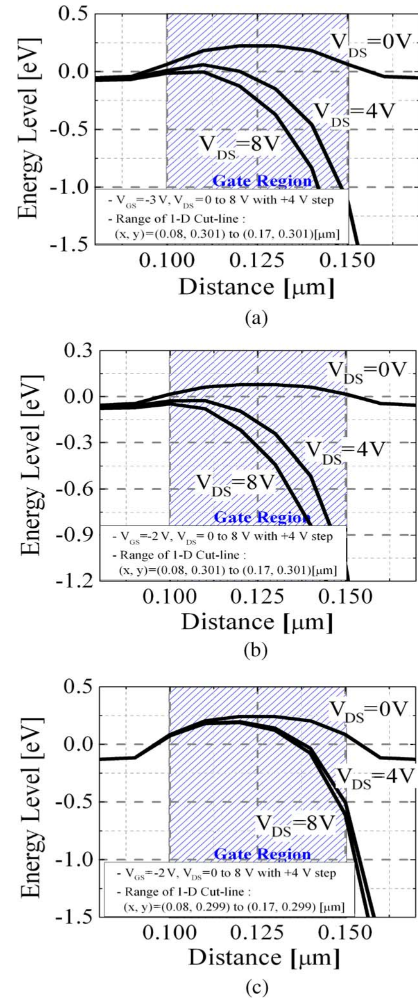

Fig. 4. Conduction energy band profiles along the channel of each HEMTs with different drain bias, which are corresponding to the solid line in Fig. 3. (a) Ga-SHEMT. (b) Ga-DHEMT. (c) N-HEMT.

applied, so that current can flow through the channel without any obstruction. This potential barrier lowering results in the threshold voltage shift and DIBL in the channel. However, N-HEMT still holds its potential barrier under a high drain bias since the gate bias directly controls the potential barrier. Thus, N-HEMT is expected to maintain good pinchoff performance and a very low output conductance unlike other two Ga-polar HEMTs.

Space charge injection also contributes to current flow under hard pinchoff conditions in Ga-HEMTs. A dash-dotted line in Fig. 3(b) shows the I–V curve of Ga-DHEMT at $V_{GS} = -3$ V, and Fig. 5(a) and (b) is the corresponding 2-D conduction band profile in the intrinsic channel layer. The applied gate bias maintains the potential barrier higher than the quasi-Fermi level to prevent the current flowing through the channel at high drain bias [inset of Fig. 5(c)]. The device, which is initially pinched off when the drain bias is low, turns on as the drain bias is increased beyond 7 V. Two vertically cut 1-D conduction band profiles show that the applied drain bias in Ga-DHEMT lowers not only the potential barrier height in the channel but also the band-engineered back barrier in Fig. 5(c). As the drain bias increases, electrons injected from source start to accumulate on the source-side gate edge of the $\mathrm{GaN/Al_{0.04}Ga_{0.96}N}$ interface. The accumulated electrons create a field opposing the back-barrier inside the channel layer. This field compensates the back-barrier structure as the drain bias increases and forms a parasitic channel at the $\mathrm{GaN/Al_{0.04}Ga_{0.96}N}$ interface. With the onset of the formation of this parasitic channel, current starts to flow through the channel formed at the bottom $\mathrm{GaN/Al_{0.04}Ga_{0.96}N}$ interface rather than the actual channel at the top $\mathrm{Al_{0.3}Ga_{0.7}N/GaN}$ interface.

The gate of N-HEMT directly controls the field in the channel layer unlike in the case of Ga-HEMTs. Since the 2-DEG channel in N-HEMT is firmly confined due to the depletion and an abrupt junction at the heterointerface, the drain field only affects the 2-DEG channel. Furthermore, since the conduction band offset at the $\mathrm{GaN/Al_{0.3}Ga_{0.7}N}$ interface creates the back-barrier structure of N-HEMT, electrostatics cannot lower the barrier structure, and electrons need much higher energy to enter the $\mathrm{Al_{0.3}Ga_{0.7}N}$ back-barrier layer in N-HEMT. N-HEMT shows better DIBL suppression compared with Ga-polar HEMTs with the same aspect ratio and the thickness of the channel layer. These advantages make N-face orientation suitable for scaled transistors. In our simulation study (not

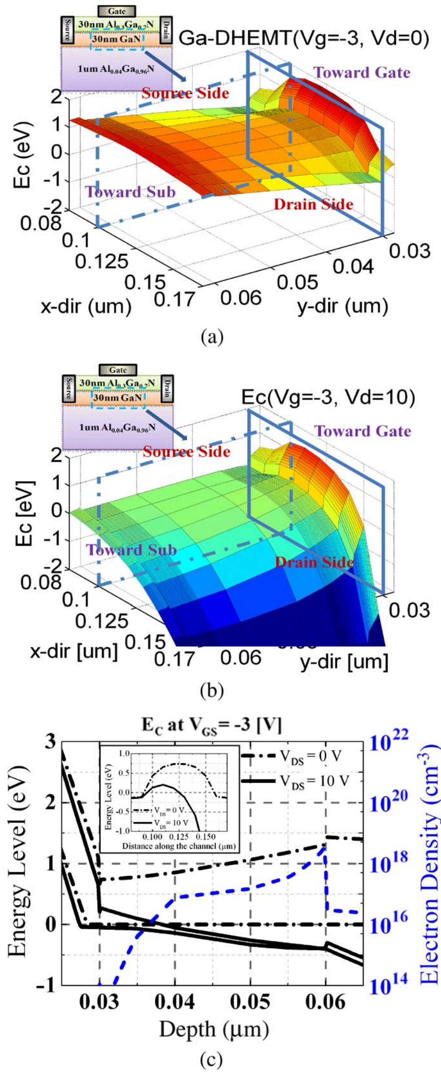

Fig. 5. One-dimensional and two-dimensional conduction band profiles in the intrinsic channel layer ($V_{GS} = -3$ V $= V_P - 1$ V, and $V_{DS} = 0$ and 10 V). (a) 2-D Conduction band profiles at $V_{DS} = 0$ V. (b) 2-D Conduction band profiles at $V_{DS} = 10$ V. (c) 1-D conduction energy band and electron density (dashed line) profiles. (Outset) Vertical cut-lines along the source-side gate edge in (a) and (b). (Inset) Lateral cut-lines along the channel in (a) and (b).

shown here), N-HEMT starts to show output conductance when the gate length shrinks down below 25 nm.

The conventional definition of DIBL (defined as $\Delta V_{\mathrm{th}}/\Delta V_{DS}$) is still useful in characterizing the threshold voltage shift in HEMT. In Fig. 6(a), Ga-DHEMT shows not only a large threshold voltage shift but also a significant degradation in the subthreshold slope unlike in the N-HEMT case. Fig. 6(b) shows the conventional DIBL as a function of the drain bias. An integration of Fig. 6(b) gives the total threshold voltage shift at a certain drain bias caused by DIBL. The space-charge-limited injection through the entire channel layer mainly contributes to short-channel effects in Ga-polar HEMTs at a high drain bias ($V_{DS} > 2.5$ V), so that a large threshold voltage shift is shown in Fig. 6(b) for Ga-DHEMT. However, N-HEMT suppresses DIBL well, as expected from the I–V characteristics and the analysis of energy band diagram.

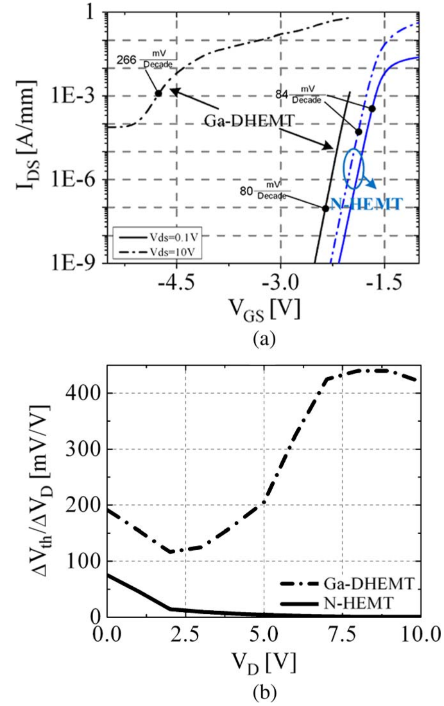

Fig. 6. Threshold voltage shift of Ga-DHEMT and N-HEMT. (a) Transfer curves for $V_{DS} = 0.1$ V (linear) and 10 V (saturation). (b) DIBL versus V_{DS}.

This nonlinear threshold voltage shift in Ga-polar HEMTs deteriorates device pinchoff and increases the output conductance of the highly scaled Ga-polar devices significantly. According to the model here, N-polar HEMTs have low output conductance and good pinchoff control as required for radio-frequency operation. We note here that real N-polar HEMTs were found to have higher output conductance, even at long gate lengths [8], [19]. Our simulations only take into account electrostatics in an idealized device. Real devices may demonstrate short-channel effects due to other nonidealities such as gate leakage current, traps, and impact ionization, which are not taken into account in this paper.

IV. Conclusion

Three different N- and Ga-polar AlGaN/GaN HEMT structures have been investigated with 1-D and 2-D conduction band profiles to compare short-channel effects due to DIBLs. Poor channel control of the two highly scaled Ga-polar HEMTs has shown the 2-D potential distribution and the space-charge-limited current flowing in a hard pinchoff condition due to short-channel effects. It has shown that an engineered double heterostructure may not fully suppress DIBLs when the applied drain bias becomes high. However, N-polar HEMT has maintained a rigorous channel confinement by its inverted HEMT structure and the direct channel control of gate, so that it exhibits superior DIBL suppression characteristics, as well as a very low output conductance with the same highly scaled condition. These results have shown that N-polar HEMTs are promising candidates for further scaling due to suppressed short-channel effects in comparison to Ga-polar HEMTs. To achieve this performance in practical N-polar HEMTs, high-κ

dielectric would be necessary to prevent gate leakage current brought from a low Schottky barrier height between gate metal and GaN while maintaining low electrical thickness of the gate insulator.

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REFERENCES

[1] Y. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm double field-plated GaN HEMTs," in *Proc. 64th Device Res. Conf.*, 2006, pp. 151–152.

[2] D. Kim, V. Kumar, J. Lee, M. Yan, A. Dabiran, A. Wowchak, P. Chow, and I. Adesida, "Recessed 70-nm gate-length AlGaN/GaN HEMTs fabricated using an Al_2O_3/SiN_x dielectric layer," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 913–915, Sep. 2009.

[3] J. W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, "AlGaN/GaN HEMT with 300-GHz $f_{\max}$," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 195–197, Mar. 2010.

[4] A. Endoh, Y. Yamashita, K. Ikeda, M. Higashiwaki, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, "Fabrication of sub-50-nm-gate i-AlGaN/GaN HEMTs on sapphire," *Phys. Stat. Sol. (C)*, no. 7, pp. 2368–2371, Dec. 2003.

[5] A. Kuliev, "0.15 μm gate-length AlGaN/GaN HEMTs with varying gate recess length," *Solid State Electron.*, vol. 47, no. 1, pp. 117–122, Jan. 2003.

[6] M. Micovic, P. Hashimoto, M. Hu, I. MilosavIjevic, J. Duvall, P. Willadsen, W. Wong, A. Conway, A. Kurdoghlian, P. Deelman, J. Moon, A. Schmitz, and M. Delaney, "GaN double heterojunction field effect transistor for microwave and millimeterwave power applications," in *IEDM Tech. Dig.*, 2004, pp. 807–810.

[7] M. Uren, K. Nash, R. Balmer, T. Martin, E. Morvan, N. Caillas, S. Delage, D. Ducatteau, B. Grimbert, and J. De Jaeger, "Punch-through in short-channel AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 395–398, Feb. 2006.

[8] S. Rajan, A. Chini, M. H. Wong, J. S. Speck, and U. K. Mishra, "N-polar GaN/AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 102, no. 4, p. 044 501, Aug. 2007.

[9] S. Dasgupta, D. F. Brown, F. Wu, S. Keller, J. S. Speck, and U. K. Mishra, "Ultralow nonalloyed Ohmic contact resistance to self aligned N-polar GaN high electron mobility transistors by In(Ga)N regrowth," *Appl. Phys. Lett.*, vol. 96, no. 14, p. 143 504, Apr. 2010.

[10] Rashmi, S. Haldar, and R. Gupta, "2-D analytical model for current-voltage characteristics and output conductance of AlGaN/GaN MODFET," *Microw. Opt. Technol. Lett.*, vol. 29, no. 2, pp. 117–123, Apr. 2001.

[11] S. Kumar, A. Agrawal, R. Chaujar, S. Kabra, M. Gupta, and R. Gupta, "Threshold voltage model for small geometry AlGaN/GaN HEMTs based on analytical solution of 3-D Poisson's equation," *Microelectron. J.*, vol. 38, no. 10/11, pp. 1013–1020, Oct./Nov. 2007.

[12] T. Palacios, S. Rajan, A. Chakraborty, S. Heikman, S. Keller, S. DenBaars, and U. Mishra, "Influence of the dynamic access resistance in the gm and fT linearity of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2117–2123, Oct. 2005.

[13] M. Farahmand, C. Garetto, E. Bellotti, K. Brennan, M. Goano, E. Ghillino, G. Ghione, J. Albrecht, and P. Ruden, "Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: Binaries and ternaries," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 535–542, Mar. 2001.

[14] J. D. Albrecht, R. P. Wang, P. P. Ruden, M. Farahmand, and K. F. Brennan, "Electron transport characteristics of GaN for high temperature device modeling," *J. Appl. Phys.*, vol. 83, no. 9, pp. 4777–4781, May 1998.

[15] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Phys. Rev. B, Condens. Matter*, vol. 56, no. 16, pp. R10 024–R10 027, Oct. 1997.

[16] J. H. Edgar, Ed., *Properties of Group III Nitrides*. London, U.K.: INSPEC, 1994.

[17] A. F. Wright, "Elastic properties of zinc-blende and wurtzite AlN, GaN, and InN," *J. Appl. Phys.*, vol. 82, no. 6, pp. 2833–2839, Sep. 1997.

[18] *Device Simulation Software, ATLAS User's Manual*, Silvaco Int., Santa Clara, CA, 2009.

[19] M. H. Wong, Y. Pei, R. Chu, S. Rajan, B. L. Swenson, D. F. Brown, S. Keller, S. P. DenBaaras, J. S. Speck, and U. K. Mishra, "N-face metal–insulator–semiconductor high-electron-mobility transistors with AlN back-barrier," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1101–1104, Oct. 2008.

[20] M. H. Wong, Y. Pei, D. F. Brown, S. Keller, J. S. Speck, and U. K. Mishra, "High-performance N-face GaN microwave MIS-HEMTs with $>70\%$ power-added efficiency," *IEEE Electron Device Lett.*, vol. 30, no. 8, pp. 802–804, Aug. 2009.

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