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# Smooth Top-Down Photoelectrochemical Etching of *m*-Plane GaN

**Adele C. Tamboli,[a,z] Mathew C. Schmidt,[a] Siddharth Rajan,[b] James S. Speck,[a] Umesh K. Mishra,[b] Steven P. DenBaars,[a] and Evelyn L. Hu[a]**

[a]*Materials Department and* [b]*Electrical and Computer Engineering Department, University of California, Santa Barbara, California 93106-9560, USA*

Photoelectrochemical (PEC) etching of *c*-plane GaN has been studied extensively because it is one of only a few available damage-free wet-etching techniques for this material system. Because of its nonpolar nature and low defect density, *m*-plane GaN may benefit from PEC etching even more than *c*-plane GaN has. With *m*-plane GaN, it is possible to achieve smooth, controllable etching, bandgap-selective top-down etching, and deep, anisotropic etching. We have investigated PEC etching of *m*-plane GaN in KOH and $HNO_3$ and have found etch rates ranging from less than 10 nm/min to more than 1 μm/min, with roughness that is crystallographic in nature but small in scale. Etch selectivity of 60:1 between $In_{0.1}Ga_{0.9}N$ and GaN is observed using PEC etching with filtered light. Anisotropic etching to depths as great as 75 μm was achieved, with the sidewall profile of the etch controlled by the direction of incident light.
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Low-damage etching is a critical device-fabrication tool for GaN materials; however, few chemical wet etches have been available for the III-nitrides.[1] Ion-damage-free wet etches could be useful for deep mesa etching, controlled recess etching for gates or contacts, and many other applications. Photoelectrochemical (PEC) etching of GaN has been studied since 1996,[2] but the major applications have been either surface roughening[3,4] or selective undercut etching of GaN structures.[5-10] The relatively high defect density of standard *c*-plane GaN typically results in rough surfaces and has made it difficult to achieve controlled top-down etching.

GaN is typically grown in the *c*-plane direction, resulting in a polarization charge and resulting electric field in the growth direction. Recently, "nonpolar" *m*-plane GaN, which is grown with the *c*-directed polarization in the plane of the sample, has shown great promise for improved optical devices including light emitting diodes (LEDs)[11] and lasers[12] because this material is not limited by the quantum-confined Stark effect, which spatially separates carriers confined in quantum wells, reducing their radiative recombination efficiency. The in-plane polarization of nonpolar *m*-plane GaN provides new design opportunities for devices such as high-electron-mobility transistors (HEMTs) and LEDs with polarized light emission. A key breakthrough in allowing the growth of *m*-plane GaN has been the development of GaN substrates grown by hydride vapor-phase epitaxy (HVPE) along the *c* direction and then sliced to expose the *m*-plane facet, allowing homoepitaxial growth of nonpolar GaN.[11,12] Growth on these substrates provides the benefit of lower defect density than GaN on sapphire because of lattice matching.[12,13] The lower defect densities and nonpolar nature of recently available *m*-plane GaN may remove some of the constraints observed for PEC etching of *c*-plane GaN. Our initial studies of top-down PEC etching of *m*-plane GaN show smooth etched surfaces and anisotropic etching, with profile of the etched sidewalls determined by the direction of incident light.

PEC etching consists of an above-bandgap light source and an electrochemical cell,[14] where the semiconductor acts as the anode and metal in contact with the surface acts as the cathode, as shown in Fig. 1. During the etch process, electron–hole pairs are generated in the semiconductor by the incident light and enhance or enable material removal. In n-type materials, photogenerated holes are pushed to the surface by bandbending at the semiconductor/electrolyte interface, where they oxidize the semiconductor surface. This oxide dissolves in the electrolyte, thus resulting in etching of the material. Electrons are extracted through a cathode deposited directly on the semiconductor surface, as shown in Fig. 1. The bandbending at p-type materials in electrolytes is such that holes are driven away from the surface; thus, p-type materials are generally resistant to PEC etching.[15] The relationship of the bandgap of the semiconductor to the wavelength of light used in PEC etching allows the possibility of selective etching. There is now an extensive body of literature on the etch mechanisms and various implementations of PEC etching of GaN[1,2,5,7,14,16-19] and GaAs.[15,20-22] If the material to be etched contains a large number of defects or traps for the photogenerated carriers, such traps may dominate the etched profile and the etch rate. This is especially relevant for GaN; in fact, Youtsey et al. used PEC etching of *c*-plane, Ga-face GaN to delineate the density of threading dislocations in the material.[16] In addition to the defect-selective nature of PEC etching of *c*-plane GaN, the built-in polarization field can influence the confinement of electrons and holes and thus has a strong effect on the etch process.[5] We have also found dramatically different etch rates for the Ga- and the N-face planes of *c*-plane GaN; the N-face GaN can exhibit a slow chemical etch rate in KOH without incident light, with pyramidal etch-stop planes $(10\bar{1}\bar{1})$, while photoenhancement is necessary to observe measurable etch rates for Ga-face GaN.[17] The etched surface of PEC-etched *c*-plane GaN is therefore a composite of decoration of defects in the material and crystallographic etching defined by the slowest-etching crystal planes, as shown in Fig. 2. This image shows the roughness characteristic of *c*-plane etches as well as two etch-resistant defects which are visible as whiskers. Etching of *c*-plane GaN does not occur in a layer-by-layer fashion. Instead, etch pits tend to form at imperfections in the material surface, and then the etch proceeds along less-etch-resistant crystal faces. Even under

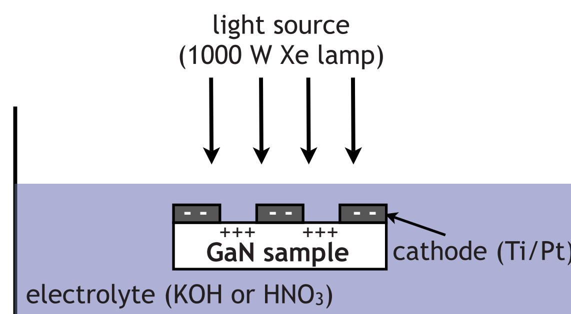


**Figure 1.** (Color online) Schematic of PEC etch apparatus used in all experiments. The semiconductor surface acts as the anode, while metal deposited directly on the surface acts as the cathode. All etches were at room temperature with no external bias applied.

[z] E-mail: atamboli@umail.ucsb.edu

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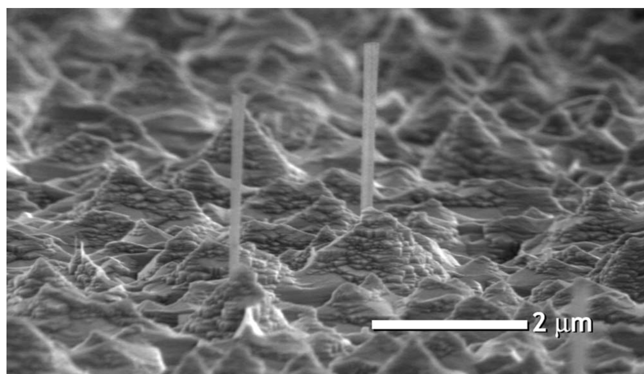


**Figure 2.** Typical etch morphology for a *c*-plane GaN sample etched in 1 M KOH. Note the roughness and the presence of etch-resistant whiskers formed around defects.

diffusion-limited conditions, which should minimize the defect- and crystallographic selectivity of the etch, it has been difficult to get controllable, smooth etches for *c*-plane GaN.

By comparison, our studies have revealed that PEC etching of *m*-plane GaN provides a highly controllable, smooth etch. Typical etch profiles shown in Fig. 3 are similar to what one might expect from PEC etching of GaAs or another III-V material having a lower defect density.[20,21] Because of the nonpolar nature and the lower defect density of *m*-plane GaN, PEC etching has the potential to become a powerful processing tool for this material system. In this work, we describe recent progress in PEC etching of *m*-plane GaN and InGaN. It is possible to achieve smooth etching that is controllable using this technique, because defects and polarization-related effects do not hinder etch smoothness. Bandgap-selective top-down etching is possible, with selectivity as high as 60:1 between $In_{0.1}Ga_{0.9}N$ and GaN. Deep, anisotropic etches up to 75 μm in depth have been achieved, with etched sidewall profiles that can be controlled by the direction of illumination during etching.

## Experimental

Epitaxial samples were grown by metallorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) on *m*-plane GaN substrates provided by Mitsubishi Chemical Corporation. The substrates were HVPE-grown *c*-plane GaN films that were sliced into *m*-plane pieces and polished with resulting root mean square (rms) roughness of less than a nanometer and a nominal n-type doping level of $5 \times 10^{17}$ $cm^{-3}$. PEC etching was performed using a variable-power Xe lamp with a nominal range of 500–1000 W and a spot size 2 in. in diameter. In all the etch studies, standard lithographic techniques followed by electron-beam deposition of 5 nm of Ti and 30 nm of Pt resulted in metal stripes patterned directly on the samples for use as both a cathode during etching and an etch mask. An optical microscope image of the mask used is shown in Fig. 4. The geometry of the metal mask is important in these experiments;[22] this mask was chosen so that the area of the cathode was similar to the area of the semiconductor to be etched, multiple trench widths could be examined (100 and 5 μm), and etched features with corners could be formed (Fig. 3a and b). No external bias was applied for any of the etches. Electrolytes used were various concentrations of KOH and $HNO_3$. All etches were performed at room temperature with no applied bias. A schematic of the etch apparatus is given in Fig. 1. Characterization was done using scanning electron microscopy (SEM), atomic force microscopy (AFM) in tapping mode, and Dektak profilometry. For etch depths reported in the Etch Rate and Roughness section, both cross-sectional SEM and Dektak were used to confirm the etch depth. Errors reported are calculated by measuring several spots on the same sample and do not account for substrate-to-substrate variation.

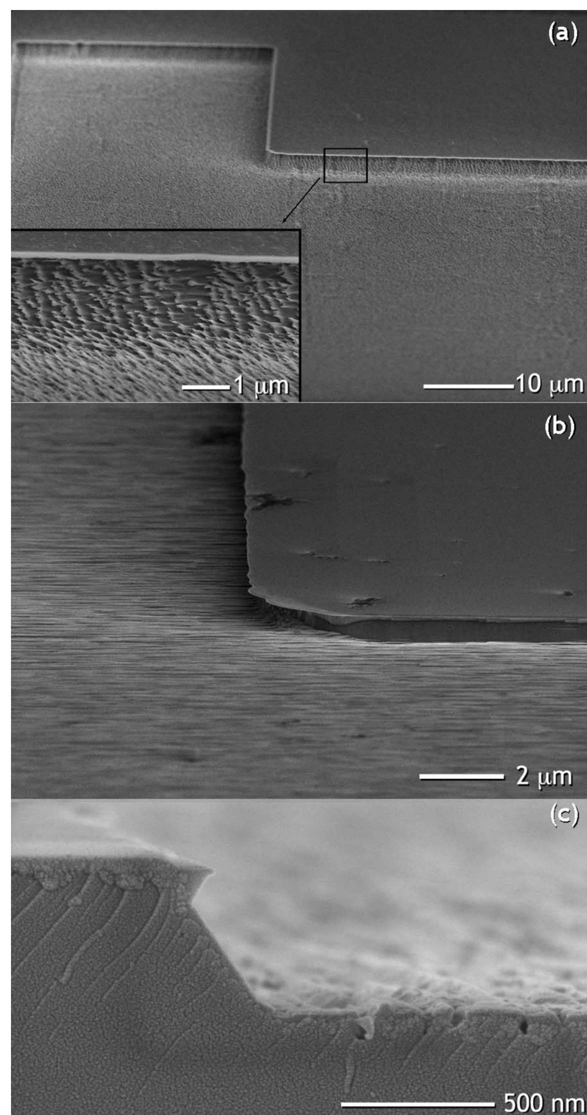


**Figure 3.** Top-down etching of *m*-plane GaN substrates: (a) sample etched in 1 M $HNO_3$, with inset showing sidewall roughness in detail, (b) sample etched in 1 M KOH, and (c) cross-sectional view of the sample etched in 1 M KOH showing a typical sidewall profile for all etches discussed in the Etch Rate and Roughness section. These samples were etched for 20 min under 1000 W illumination.

## Results and Discussion

*Etch rate and roughness.*— HVPE-grown *m*-plane GaN substrates were used to investigate the general properties of PEC etching of *m*-plane GaN. After metallization and liftoff, samples were etched for 20 min each in a variety of different etchants and with the Xe lamp power set to either 500 or 1000 W. Most etches were done at a high power (nominally 1000 W) to produce a fairly smooth etch in the reaction-rate-limited regime; however, one set of etches was done at lower power (nominally 500 W) to examine the variation possible with different illumination intensities. All etches were done with unfiltered light, and the solutions were not stirred, although stirring can often produce a smoother etched surface. All concentrations of KOH and $HNO_3$ studied yield smooth etching, as shown in Fig. 3. Figure 3a shows a sample etched in 1 M $HNO_3$ at a power of 1000 W, with typical morphology for a $HNO_3$ etch in the concentration range studied. There is some crystallographically oriented roughness, which is reminiscent of the growth morphology for *m*-plane GaN grown on on-axis substrates.[23] Although the roughness

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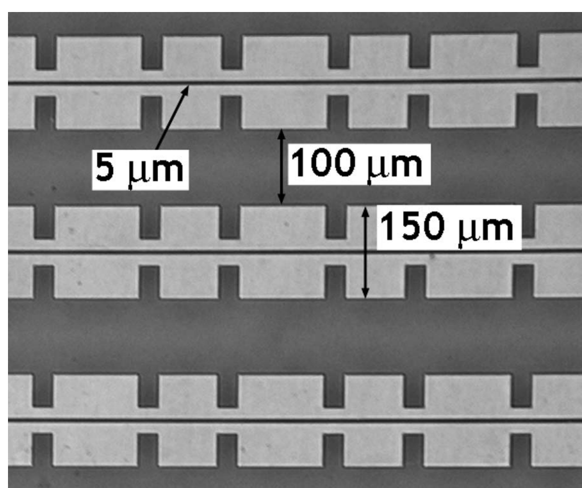


**Figure 4.** Mask used for metal cathode pattern during etch studies, with dimensions of metal stripes and spacings between stripes labeled.

is oriented in the c-direction, there are no crystallographic facets defined by the etch, and it is likely that the morphology may reflect the mode of growth of the substrate material. The magnitude of the rms roughness is low, as measured by a 10 × 10 μm AFM scan; for a 1.7 μm deep etch, the rms roughness is 55 nm. Overall, the etched morphology is almost completely controlled by the illumination. Figure 3b shows a similar image for a sample etched at 1000 W in 1 M KOH. In this case, the rms roughness is 30 nm for an etch depth of 0.5 μm. Again, this etch morphology is typical for a KOH etch in the concentration range studied, and an interesting feature of this etch is that there are striations visible in the *c* direction. These striations are probably caused by threading dislocations from the HVPE growth, because defects etch at a reduced rate under most PEC etch conditions.[16] Figure 3c shows a cross-sectional SEM image of the sample from Fig. 3b, which illustrates a typical sidewall profile seen in all of the KOH and $HNO_3$ etches performed. The etched sidewall is sloped with an angle that becomes steeper as the etch gets deeper, eventually resulting in a strongly anisotropic etch profile, as discussed in the Deep Etching section.

A summary of etch depths and roughness for a variety of etchant concentrations can be found in Fig. 5. Etch rates are given in Table I. These etch rates are time averages for a 20 min etch and do not account for the time lag for etching to start, so they may not apply to short etches. In the case of $HNO_3$, etch depth generally increases with etchant concentration for 1000 W illumination. For $HNO_3$ at 500 W, etch rates were weakly dependent on etchant concentration,

**Table I. Etch rates for various etch conditions, in nanometers per minute.**

| | KOH, 1000 W | $HNO_3$, 1000 W | $HNO_3$, 500 W |
|---|---|---|---|
| 1 M | 28 ± 1 | 86 ± 3 | 23 ± 1 |
| 0.2 M | | | 34 ± 1 |
| 0.1 M | 34 ± 3 | 54 ± 1 | 16 ± 3 |
| 0.01 M | 41 ± 4 | 44 ± 1 | 17 ± 1 |
| 0.001 M | 154 ± 16 | 8 ± 2 | |

probably because at that lower power most of these etches are in a carrier-limited regime, where traps play a more significant role. The KOH etches follow the opposite trend, with etch rate increasing as concentration decreases. Other groups have also observed this trend at high KOH concentration.[18] Roughness (Fig. 5b) generally follows the same trends as etch depth except for an anomalous point at 0.001 M KOH. This sample was etched deeply (>3 μm) and had a low rms roughness of about 20 nm, although the etched trench exhibited an inverted U shape; the etch depth was greatest nearest to the metal mask and shallower in the center of the trench. This etch profile could result from variations in hole concentration as a function of distance from the cathodic metal mask, because recombination is reduced where electrons are most efficiently extracted.[22] A related effect has been observed when using damage-induced masking for PEC etching of GaAs.[24] The etch depth we report here was measured at the edge of the mask, where the depth was greatest, but ranged to as low as 650 nm near the center of some of the wider metal-stripe spacings (100 μm) and was close to uniformly 3 μm deep between metal stripes with more narrow (5 μm) spacing.

*Bandgap-selective etching*.— PEC etching is inherently bandgap-selective. It has been well established that InGaN layers can be etched selectively in GaN/InGaN/AlGaN heterostructures by passing the incident light through a GaN filter.[5] With this technique, we have been able to form optical and electronic devices by the selective undercut of sacrificial InGaN layers.[5,6,9,10] For top-down etching, bandgap selectivity could allow us to incorporate etch-stop layers to stop smoothly on a particular layer, which would have many applications, including the fabrication of microcavity LEDs[25] and gate-recessed HEMTs.[26-29] Because it has been difficult in the GaN-material system to achieve high selectivity using dry etching,[25,29] PEC etching is especially important for these applications. The ion-damage-free nature of PEC etching also ensures the quality of the active region for these devices.

To test the selectivity of PEC etching, we used an MBE-grown sample that consisted of 200 nm of $In_{0.1}Ga_{0.9}N$ grown on an n-type GaN substrate. As in the previous section, we used a Ti/Pt cathode

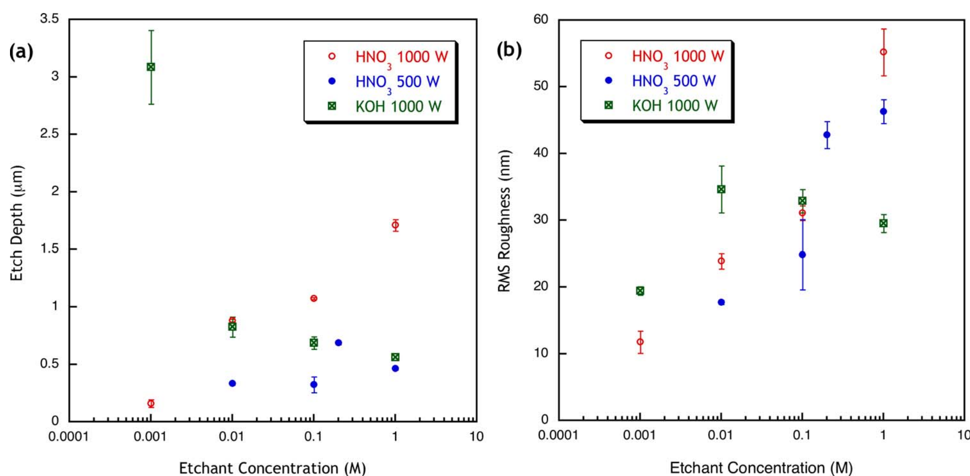


**Figure 5.** (Color online) Etch depth and rms roughness for samples etched for a total of 20 min. KOH and $HNO_3$ are used as electrolytes, and the lamp power is set to 500 or 1000 W, unfiltered, and unfocused.

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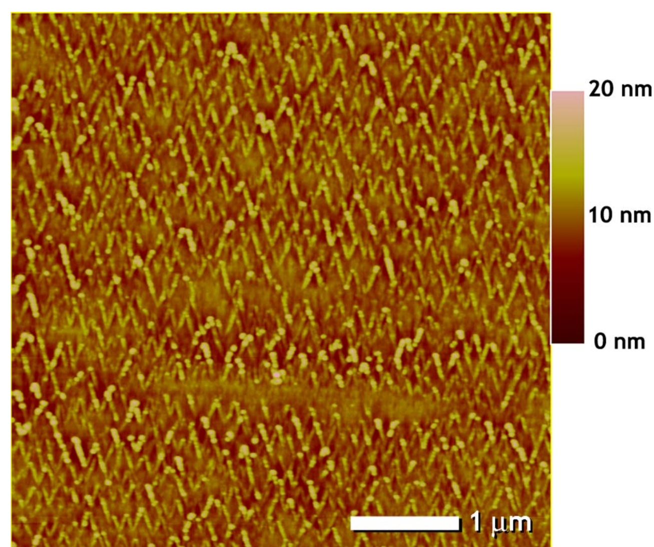


**Figure 6.** (Color online) AFM image of the GaN surface exposed by a bandgap-selective etch of an InGaN layer. The etch stopped smoothly on the GaN, as evidenced by the 20 nm height scale and low rms roughness of less than 2 nm. The *c* axis is vertical in this image.

deposited directly on the sample. PEC etching was performed with a GaN filter at 1000 W in 0.01 M $HNO_3$ for 15 min to 3 h. The InGaN layer was completely etched away after 20 min, and the etch stopped on the GaN. Figure 6 shows a 5 × 5 μm AFM scan of the resulting GaN surface. The height scale in this image is 20 nm, and the rms roughness is less than 2 nm, which is smaller than the roughness of the as-grown InGaN. The resulting etch rate of InGaN was 94 ± 2 Å/min, and the etch rate of GaN was 1.59 ± 0.04 Å/min, resulting in a selectivity of 60:1. The etch rate for InGaN reported here is much lower than for GaN using the same etchant (Table I, 44 ± 1 nm/min) because we are using a GaN filter, eliminating the high-energy component of the lamp spectrum completely, which results in only the narrow band of energy between the bandgaps of GaN and $In_{0.1}Ga_{0.9}N$ being absorbed for etching.

*Deep etching*.— For many device applications, deep, anisotropic etches are required. PEC etching has had limited results in the GaN system thus far because the resulting etch morphology is rough when *c*-plane GaN is used. *M*-plane GaN substrates and templates, however, can be etched directly using PEC etching. Rapid etches can be achieved by increasing both the electrolyte concentration and the light intensity, resulting in a reaction-rate-limited etch.

We have been able to achieve deep, anisotropic etches using *m*-plane GaN substrates (Fig. 7). For this study, we used a GaN template layer a few micrometers thick grown by MOCVD on a GaN substrate, with Ti/Pt deposited as described above. PEC etching was performed in 1 M $HNO_3$ for 1 h with the lamp set to 1000 W and focused to a spot size of about a square centimeter, resulting in a power density about 25 times as high as that used for the etches in the preceding sections. The resulting etch profile can be seen in Fig. 7. The etch depth obtained was about 75 μm near the center of the lamp spot, where the light was brightest, corresponding to an etch rate of 1.3 μm/min. Using these etch conditions, a substrate could be removed in a few hours. It can also be seen from Fig. 7b that the GaN template layer visible at the surface of the material etches more slowly than the substrate. This sample is an unintentionally doped (uid) substrate (doping level $5 \times 10^{17}$ $cm^{-3}$) with a two-layer epitaxial template, with the first layer being a uid ($5 \times 10^{16}$ $cm^{-3}$) GaN layer and the second an n-type ($5 \times 10^{18}$ $cm^{-3}$) GaN layer. The layer visible at the top in Fig. 7b is the n-type GaN layer, and the underlying uid GaN layer is also

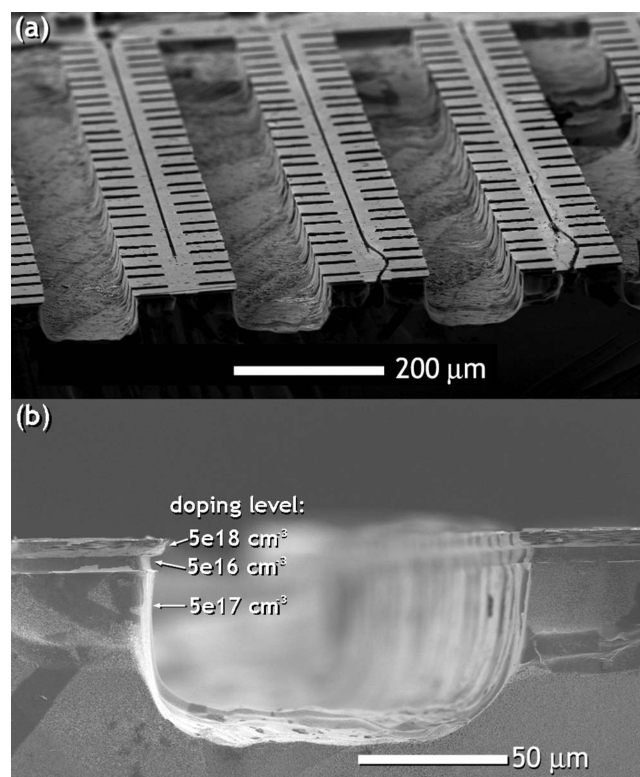


**Figure 7.** Deep top-down etch of an m-GaN sample: (a) an overview of the sample, showing good overall smoothness and uniformity for an etch this deep, and (b) a cross-sectional view of the same sample, showing the anisotropic nature of the etch. The thin etch mask is not visible, but three layers with different doping levels are labeled: the n-type substrate, an unintentionally doped epitaxial layer, and an n-type epitaxial layer.

visible because it etched slightly faster than the uid substrate. The etch rate of n-type GaN decreased as the doping level increased,[18,19] because etching is driven by minority carriers.

Figure 8 shows a sample etched with the light directed to the substrate at an angle of 55°. In this case, the sample was mounted such that the left side of the sample was higher than the right and the lamp was directly above. The top (left) edge, which is shown in detail in Fig. 8c, has a sloped sidewall characteristic of the angle of the incident light. The lower (right) sidewall is also angled, but there is some undercutting of the mask, probably caused by unintentional reflections in the etch setup. Etching was performed in a Pyrex beaker which easily scatters light. This experiment shows that the etched profile can be controlled by manipulating the incident light.

## Conclusions

We have demonstrated the broad applicability of PEC etching to nonpolar III-nitride device fabrication. PEC etching can be used for smooth, controllable etching in a variety of concentrations of KOH and $HNO_3$ with etch rates up to 1.3 μm/min. It is possible to incorporate an etch-stop layer, with selectivity of 60:1 between $In_{0.1}Ga_{0.9}N$ and GaN, to get smooth, precise etching for devices with critical dimensions. Finally, we have been able to etch deep, smooth, anisotropic trenches in a controllable manner, with etch depths up to 75 μm, and we have shown that the anisotropic etch profile can be manipulated by changing the direction of incident light during the etch. These results show that PEC etching could lead to improved performance in nonpolar devices when ion damage or device size is critical.

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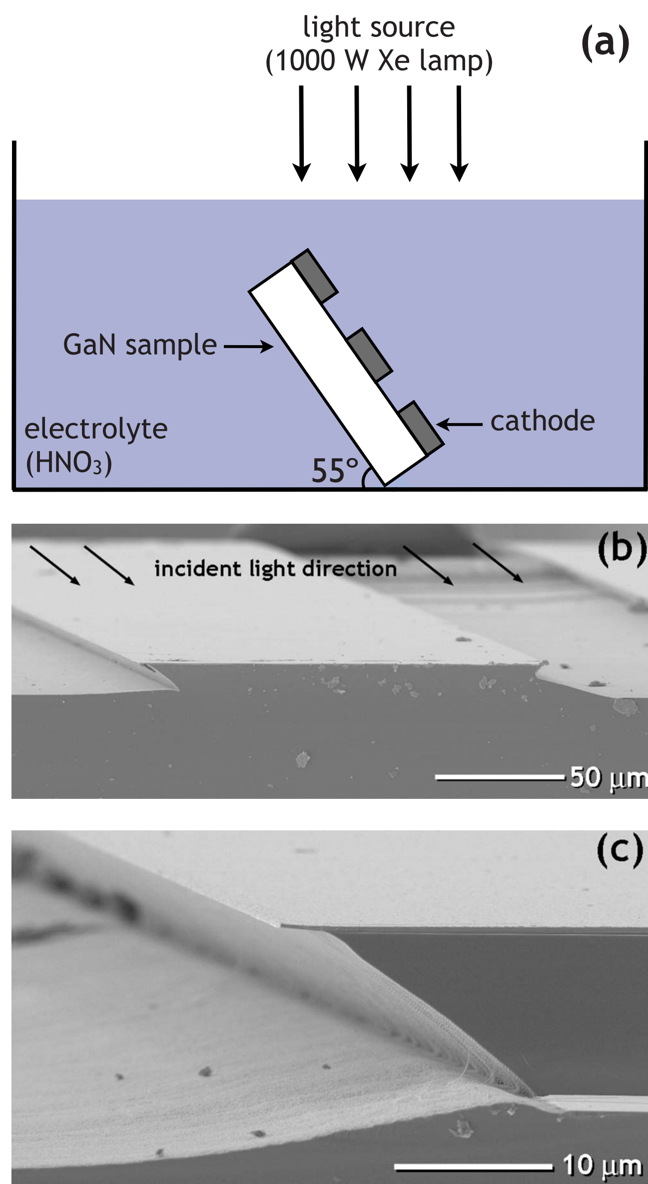


**Figure 8.** (Color online) (a) Schematic of etch apparatus used for angled illumination. (b) Etched profile resulting from light incident at an angle of 55° from the sample surface normal. The sidewall angle is determined by the directionality of the incident light, although there is some undercut on the right (bottom) side caused by reflections in the etch setup. The etch mask is visible in the higher-magnification image (c) and shows a slightly undercut mask.


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## References


1. D. Zhuang and J. H. Edgar, *Mater. Sci. Eng., R.*, **48**, 1 (2005).
2. M. S. Minsky, M. White, and E. L. Hu, *Appl. Phys. Lett.*, **68**, 1531 (1996).
3. Y. Gao, T. Fujii, R. Sharma, K. Fujito, S. P. DenBaars, S. Nakamura, and E. L. Hu, *Jpn. J. Appl. Phys., Part 2*, **43**, L637 (2004).
4. L. Zhou, J. E. Epler, M. R. Krames, W. Goetz, M. Gherasimovam, Z. Ren, J. Han, M. Kneissl, and N. M. Johnson, *Appl. Phys. Lett.*, **89**, 241113 (2006).
5. E. D. Haberer, R. Sharma, A. R. Stonas, S. Nakamura, S. P. DenBaars, and E. L. Hu, *Appl. Phys. Lett.*, **85**, 762 (2004).
6. Y. Gao, I. Ben-Yaacov, U. K. Mishra, and E. L. Hu, *J. Appl. Phys.*, **96**, 6925 (2004).
7. B. Yang and P. Fay, *J. Vac. Sci. Technol. B*, **24**, 1337 (2006).
8. C.-F. Lin, Z.-J. Yang, B.-H. Chin, J.-H. Zheng, J.-J. Dai, B.-C. Shieh, and C.-C. Chang, *J. Electrochem. Soc.*, **153**, G1020 (2006).
9. R. Sharma, E. D. Haberer, C. Meier, E. L. Hu, and S. Nakamura, *Appl. Phys. Lett.*, **91**, 211108 (2007).
10. A. C. Tamboli, E. D. Haberer, R. Sharma, K. H. Lee, S. Nakamura, and E. L. Hu, *Nat. Photonics*, **1**, 61 (2007).
11. M. C. Schmidt, K.-C. Kim, H. Sato, N. Fellows, H. Masui, S. Nakamura, S. P. DenBaars, and J. S. Speck, *Jpn. J. Appl. Phys., Part 2*, **46**, L126 (2007).
12. M. C. Schmidt, K.-C. Kim, R. M. Farrell, D. F. Feezell, D. A. Cohen, M. Saito, K. Fujito, J. S. Speck, S. P. DenBaars, and S. Nakamura, *Jpn. J. Appl. Phys., Part 2*, **46**, L190 (2007).
13. K. Okamoto, H. Ohta, D. Nakagawa, M. Sonobe, J. Ichihara, and H. Takasu, *Jpn. J. Appl. Phys., Part 2*, **45**, L1197 (2006).
14. C. Youtsey, I. Adesida, and G. Bulman, *Appl. Phys. Lett.*, **71**, 2151 (1997).
15. J. van de Ven and H. J. P. Nabben, *J. Electrochem. Soc.*, **138**, 3401 (1991).
16. C. Youtsey, L. T. Romano, and I. Adesida, *Appl. Phys. Lett.*, **73**, 560 (1998).
17. Y. Gao, M. D. Craven, J. S. Speck, S. P. DenBaars, and E. L. Hu, *Appl. Phys. Lett.*, **84**, 3322 (2004).
18. H. Cho, K. H. Auh, J. Han, R. J. Shul, S. M. Donovan, C. R. Abernathy, E. S. Lambers, F. Ren, and S. J. Pearton, *J. Electron. Mater.*, **28**, 290 (1999).
19. B. Yang and P. Fay, *J. Vac. Sci. Technol. B*, **22**, 1750 (2004).
20. J. van de Ven and H. J. P. Nabben, *J. Electrochem. Soc.*, **137**, 1603 (1990).
21. J. van de Ven and H. J. P. Nabben, *J. Electrochem. Soc.*, **138**, 144 (1991).
22. R. Khare, E. L. Hu, J. J. Brown, and M. A. Melendes, *J. Vac. Sci. Technol. B*, **11**, 2497 (1993).
23. A. Hirai, Z. Jia, M. C. Schmidt, R. M. Farrell, S. P. DenBaars, S. Nakamura, J. S. Speck, and K. Fujito, *Appl. Phys. Lett.*, **91**, 191906 (2007).
24. R. Khare and E. L. Hu, *J. Appl. Phys.*, **72**, 1543 (1992).
25. Y.-S. Choi, M. Iza, E. Matioli, G. Koblmüller, J. S. Speck, C. Weisbuch, and E. L. Hu, *Appl. Phys. Lett.*, **91**, 061120 (2007).
26. A. T. Ping, D. Selvanathan, C. Youtsey, E. Piner, J. Redwing, and I. Adesida, *Electron. Lett.*, **35**, 2140 (1999).
27. W. S. Lee, Y. H. Choi, K. W. Chung, D. C. Moon, and M. W. Shin, *Electron. Lett.*, **36**, 265 (2000).
28. H. Maher, D. W. DiSanto, M. W. Dvorak, G. Soerensen, C. R. Bolognesi, J. A. Bardwell, H. Tang, and J. B. Webb, *Electron. Lett.*, **36**, 1969 (2000).
29. Y. Pei, L. Shen, T. Palacios, N. A. Fichtenbaum, L. S. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, *Jpn. J. Appl. Phys., Part 2*, **46**, L842 (2007).


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