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TRAP BEHAVIOR IN AlGaN/GaN HEMTs BY POST-GATE-ANNEALING

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Trapping effects are investigated to examine the post-gate annealing effects on AlGaN/GaN high-mobility electron transistors (HEMTs) using pulsed I-V and transient measurements. In the unannealed devices, shallow traps are identified, which have an activation of 38 meV at a drain bias of 7 V. The time constant of these traps is determined to be ~0.5 μs. Devices annealed at 400 °C for 10 minutes have a significantly smaller number of traps. However, a small number of traps with a longer time constant of 9.2 μs are created or activated during post-gate annealing. 20-minute annealing at 400 °C leads to the increase of the number of traps with emission time constants of 21.6 μs and 1.25 ms. The breakdown voltage improvement by post-gate annealing is attributed to the removal or significant reduction of the shallow level traps.

1 Introduction

GaN-based high electron mobility transistors (HEMTs) have great potential for high power and high frequency applications because of their inherent material nature as demonstrated recently.[1-3] However, critical issues including current dispersion and device reliability have limited the AlGaN/GaN HEMTs for practical applications. Current dispersion due to trapping effects associated with these devices causes decrease in the actual output drain current and voltage swing at RF operations.[4] To reduce the trapping effects, several approaches on device fabrication process and material growth have been performed including: e.g., surface passivation, a thin AlN barrier layer in AlGaN/GaN interface, application of a field plate, and Si doping on GaN/AlGaN/GaN heterostructures.[3, 5-7] Moreover, attempts to increase in breakdown voltage have been made by using a field plate and gate dielectrics.[8] Recently, we demonstrated that post-gate-annealing (PGA) process can improve AlGaN/GaN HEMTs dramatically in gate leakage current, breakdown voltage performance,[9] and even the maximum drain current under an optimized processing condition. These phenomena are mostly related to traps due to imperfection of the AlGaN/GaN heterostructures. Thus, investigations of trapping effects are of importance for any novel processing techniques for high performance AlGaN/GaN HEMTs.[10] In this paper, trapping effects are investigated to understand effects of the post-gate annealing, using short drain current transient and static/dynamic current-voltage (I-V) measurements.

2 Device Fabrication and Pulsed Measurement Methods

The AlGaN/GaN HEMT epilayer structure was grown by metal-organic chemical vapor deposition on a SiC substrate. The epilayer consists of 40 nm AlN nucleation layer, 3 μm of undoped GaN, and 20 nm undoped $Al_{0.3}Ga_{0.7}N$. Device fabrication procedures follow

the standard process such as mesa isolation by dry etching, Ti/Al/Mo/Au ohmic contact metallization by electron beam evaporation and rapid thermal annealing, and Ni/Au Schottky gate with a gate-length of 0.2 μm by electron beam lithography. The devices have a gate width of 100 μm and a source to drain spacing of 3 μm. To investigate PGA effects on AlGaN/GaN HEMTs, the wafer was cleaved to three samples. Sample 1 was not annealed for reference. Samples 2 and 3 were annealed at 400 °C for 10 and 20 minutes, respectively, in a furnace with N_2 ambient. After annealing, the breakdown voltage of the annealed samples 2 and 3 increased dramatically from ~ 35 V to higher than 180 V. The maximum drain current of sample 2 in the DC I-Vs had improvement but the sample 3 had slightly degradation in comparison with the reference sample [9, 11]. The pulsed I-Vs are characterized at different QB conditions; (V_{DS0}, V_{GS0}) = (0 V, 0 V), (0 V, -5 V), and (7 V, -5 V) as shown in Fig. 1. Under these three QBs, there is essentially no drain current flowing in the channel. Electrons are depleted at QBs of (V_{DS0}, V_{GS0}) = (0 V, -5 V) and (7 V, -5 V) and some of them are trapped, while there is no electron trapping at (V_{DS0}, V_{GS0}) = (0 V, 0 V). The pulse widths (PWs) of 200 ns, 500 ns, 10 μs, and 100 μs are used with a pulse separation of 1 ms. The DC and pulsed I-V curves measured at V_{GS} = 0 V are used to investigate the trapping behavior of three samples.

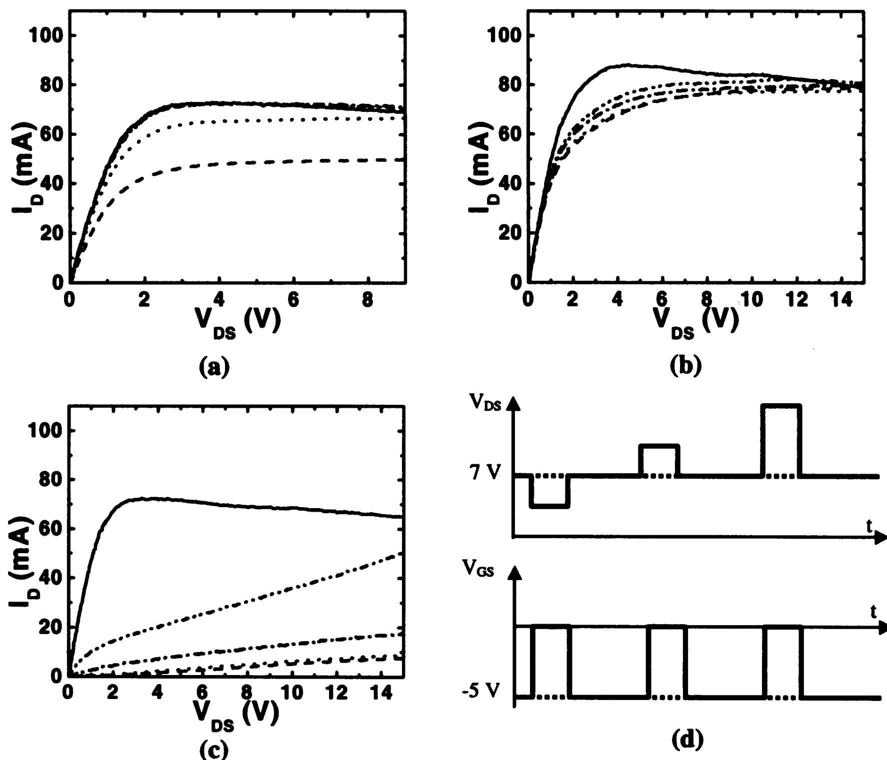

Fig. 1. DC I-V (solid) and pulsed I-V at V_{GS} = 0V and a quiescent bias point of (V_{DS0}, V_{GS0}) = (7 V, -5 V) at pulse widths of 0.2 μs (dash), 0.5 μs (dot), 10 μs (dash dot), and 100 μs (dash dot dot). [pulse separation: 1ms]: (a) unannealed HEMTs, HEMTs annealed at 400°C for 10 minutes (b) & 20 minutes (c), and (d) bias conditions

3 Results and Discussion

Figure 1 shows DC I-V and pulsed I-V with different pulse widths at V_{GS} = 0 V at a quiescent bias point of (V_{DS0}, V_{GS0}) = (7 V, -5 V). Under this quiescent bias, some electrons are captured by traps. At a longer pulse width, the drain current in pulsed I-Vs of each sample increases. If the pulse width is shorter than the emission time constant (t_E), electrons captured by traps do not have enough time to be fully emitted. But if the pulse width is long enough, all the trapped electrons are detrapped and contribute to drain current. The current dispersion between DC and the 0.2 μs pulsed I-Vs in the unannealed HEMTs (Fig.1(a)) is much larger than that in the 10-minute annealed devices, indicating a larger number of traps are removed during the post-gate annealing. The difference between DC I-V and 10/100 μs pulse I-V curves in the unannealed devices is negligible. But I_D dispersion in the annealed samples 2 and 3 is observed, which suggests that a small number of traps with a long time constant are created during the post-gate annealing, though the total number of traps is significantly smaller than that of unannealed devices. In 100 μs pulsed I-Vs, severer current dispersion in 20-minute

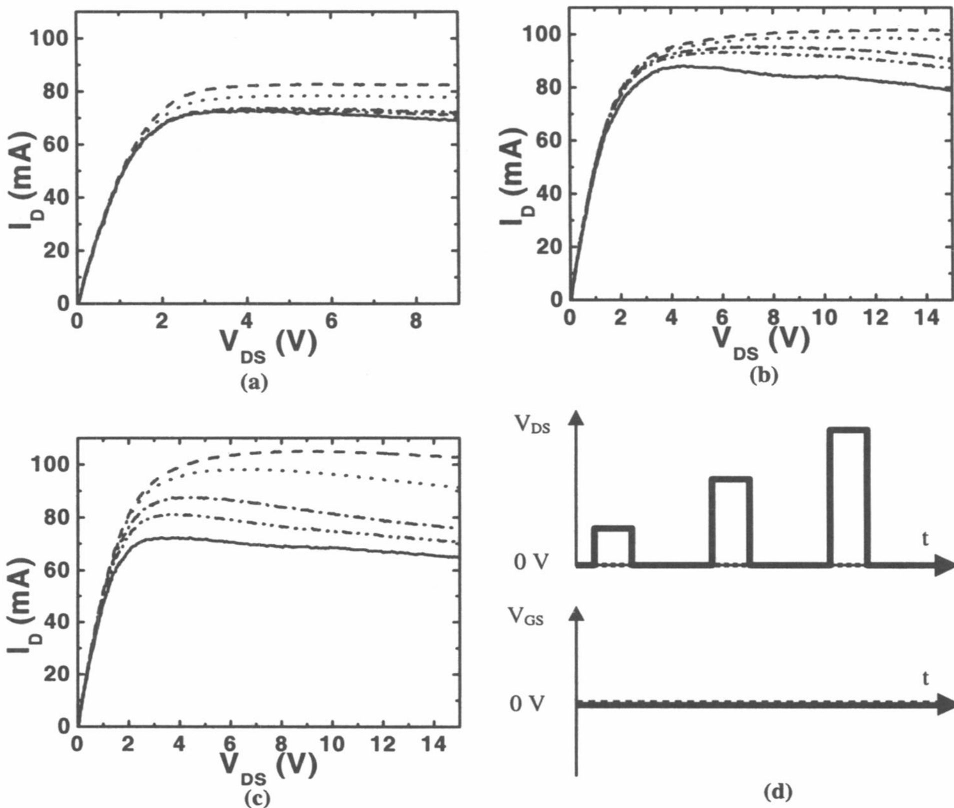

Fig. 2. DC I-V (solid) and pulsed I-V at V_{GS} = 0V and a quiescent bias point of (V_{DS0}, V_{GS0}) = (0 V, 0 V) at pulse widths of 0.2 μs (dash), 0.5 μs (dot), 10 μs (dash dot), and 100 μs (dash dot dot). [pulse separation: 1ms]: (a) unannealed HEMTs, HEMTs annealed at 400°C for 10 minutes (b) & 20 minutes (c), and (d) bias conditions

annealed HEMTs indicates that further annealing creates a much larger density of traps with a long time constant.

Fig. 2 shows DC and pulsed I-V characteristics at V_{GS} = 0 V and a quiescent bias point of (V_{DS0}, V_{GS0}) = (0 V, 0 V) with different pulse widths. As the pulse width increases, decrease in the saturation drain current is observed in the pulsed I-Vs of three samples, due to longer time available for electrons to be captured by traps. Dispersion of the saturation current between the 0.2 μs pulsed I-V and DC I-V of sample 1 and 2 is smaller than that of sample 3. This suggests that the devices annealed at 400 °C for 20 minutes have a much larger density of traps with a capture time constant (t_C) of longer than 0.2 μs. The dispersion between 10 ~ 100 μs pulsed I-Vs and DC I-Vs are observed in both annealed HEMTs. Again, this indicates that the post-gate annealing remove traps with a short capturing time constant and creates traps with a long capturing time constant.

Fig. 3 shows short drain current transient normalized by DC drain current (I_{DC}) at (V_{DS}, V_{GS}) = (7 V, 0 V). The bias was pulsed up from at (V_{DS}, V_{GS}) = (7 V, -5 V) to (7 V, 0 V). The unannealed devices show the clear transient within a few μs after pulsing-up. Based on these transient measurements, emission time constants are extracted using the following exponential decay functions:

$$I_D(t) = I_{DC}(1 - I_0 \exp[-t/\tau]) . \quad (1)$$

$$I_D(t) = I_{DC}(1 - I_1 \exp[-t/\tau_1] - I_2 \exp[-t/\tau_2]) . \quad (2)$$

where I_{DC} is the DC drain current at (V_{DS}, V_{GS}) = (7 V, 0 V), τ is time constant. The transient spectra of unannealed devices and 10-minute annealed devices fit well to Eq. (1). The transient behavior of devices annealed for 20 minutes show better fitting to Eq. (2) with double exponential decay functions. The extracted time constants of the unannealed and 10-minute annealed devices are ~ 0.5 μs and ~ 9.2 μs, respectively. The 20-minute annealed devices have emission time constants of ~ 21.6 μs and ~ 1.25 ms. These extracted time constants show clearly that the post-annealing process removes traps with a short t_E and induces traps with longer t_E.

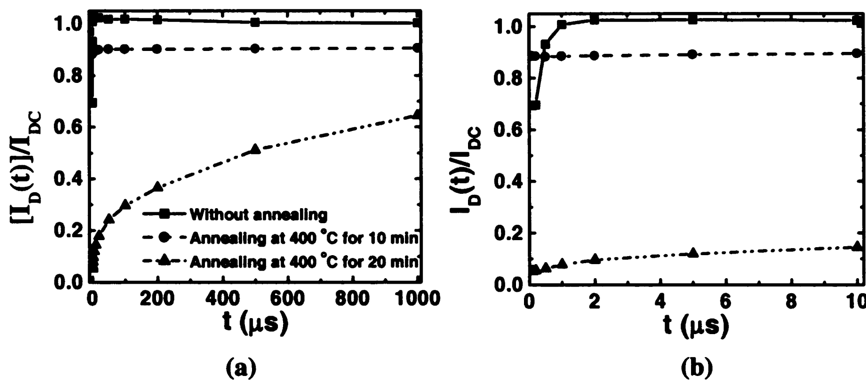

Fig. 3. (a) Normalized transient characteristics of the unannealed HEMTs (solid line), and HEMTs annealed at 400°C for 10 minutes (dashed line) & 20 minutes (dash-dot-dot line) and (b) transients in the first 10 μs. The biases are pulsed up from (V_{DS0}, V_{GS0}) = (7 V, -5 V) to (V_{DS}, V_{GS}) = (7 V, 0 V).

Fig. 4 shows normalized drain current transient of AlGaN/GaN HEMTs annealed at different conditions. The biases were pulsed down from (V_{DS0}, V_{GS0}) = (7 V, 0 V) to (V_{DS}, V_{GS}) = (7 V, -3 V). The unannealed and 10-minute annealed HEMTs don't exhibit exponential capturing process. This may be because the traps have extremely short capture time constants. However, the 20-minute annealed HEMTs show exponential decay electron capturing process. The capture time constants of ~ 0.85 μs, ~21 μs, and ~2.2 ms are extracted by fitting to a triple exponential decay function.

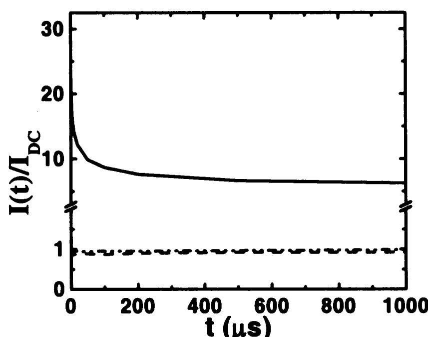

Fig. 4. (a) Normalized transient characteristics of the unannealed HEMTs (dashed line), and HEMTs annealed at 400°C for 10 minutes (dash-dot-dot line) & 20 minutes (solid line). The biases are pulsed up from (V_{DS0}, V_{GS0}) = (7 V, 0 V) to (V_{DS}, V_{GS}) = (7 V, -3 V).

Fig. 5 shows a typical short emission transient curve at room temperature and the temperature dependence of the emission time constant in the unannealed HEMTs measured from 295 K to 363 K. The temperature-dependence of t_E is shown by using the classical Arrhenius equation:

$$\tau^{-1} = CT^2 \exp(-E_A/kT)\,. \quad (3)$$

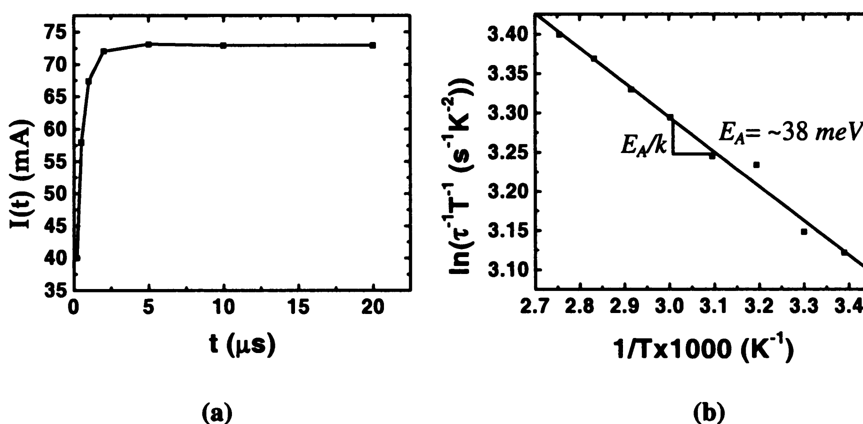

Fig. 5. (a) Typical short transient characteristic of the unannealed devices at 295 K; and (b) temperature dependence of the time constant extracted from the drain current transient curves at temperatures ranging from 295 K to 363K. The gate is pulsed from V_{GS0} = -5 to V_{GS} = 0 V and the drain voltage is 7 V.

where T is the temperature in Kelvin, E_A is the activation energy, τ is the time constant, k is the Boltzmann constant, and C is a fitting factor. The extracted activation energy of those traps with short time constants is determined to be ~ 38 meV at an electric field of 0.35 MV/cm. Such shallow level traps result in the current dispersion and a low breakdown voltage of the unannealed HEMTs. So, the significant improvement in breakdown voltage of the annealed devices is attributed to the removal of these shallow traps during the post-gate annealing.

4 Conclusions

We have investigated the post-gate annealing effects on electron capturing and emission processes of AlGaN/GaN HEMTs using dynamic and transient measurements. In the unannealed HEMTs, traps have a low activation energy of ~38 meV at V_D = 7 V. The emission time constant of these traps is about 0.5 μs. After annealing, a significantly smaller number of these shallow traps are removed. However, a small number of traps with longer emission time constants (9.2 μs for devices annealed at 400 °C for 10 minutes, and 21.6 μs and 1.25 ms for devices annealed at 400 °C for 20 minutes) are created. The breakdown voltage improvement by post-gate annealing is attributed to the removal of the shallow level traps.

Acknowledgements

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References

1. W. Lu, et al., "AlGaN/GaN HEMTs on SiC with over 100 GHz f_T and low microwave noise," *IEEE Trans. Electron Dev.* **48** (2001) 581-585.
2. V. Kumar, et al., "AlGaN/GaN hemos on SiC with f_T of over 120 GHz," *IEEE Electron Dev. Lett.* **23** (2002) 455-457.
3. Y.-F. Wu, et al., "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Dev. Lett.* **25**, (2004) 117-119.
4. C. Nguyen, et al., "Drain current compression in GaN MODFETs Ander large-signal modulation at microwave frequencies," *Electron. Lett.* **35** (1999) 1380-1382.
5. Y. Ohno, et al., "Effects of surface passivation on breakdown of AlGaN/GaN high-electron-mobility transistors," *Appl. Phys. Lett.* **84**, (2004) 2184-2186.
6. J. S. Lee, et al., "Reduction of current collapse in AlGaN/GaN HFETs using AlN interfacial layer," *Electron. Lett.* **39**, (2003) 750-752.
7. O. Mitrofanov, et al., "Impact of Si doping on radio frequency dispersion in unpassivated GaN/AlGaN/gaN high-electron-mobility transistors grown by plasma-assisted molecular-beam epitaxy," *Appl. Phys. Lett.* **82**, (2003) 4361-4363.
8. Z. Y. Fan, et al., "Delta-doped AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistors with high breakdown voltages," *Appl. Phys. Lett.*, vol. **81** (2002) 4649-4651.
9. J. Lee, et al., "Post Annealing Effects on Device Performance of AlGaN/GaN HFETs," *Solid State Electron.* **48** (2004) 1855-1859.
10. S. De Meyer, et al., "Mechanism of power density degradation due to trapping effects in AlGaN/GaN HEMTs," *Microwave Symposium Digest, IEEE MTT-S Digest* **1** (2003) 455-458.
11. J. Lee, et al., Submitted to Applied Physics Letters.