Solid-State Electronics 54 (2010) 1291–1294

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Turn-on voltage engineering and enhancement mode operation of AlGaN/GaN high electron mobility transistor using multiple heterointerfaces

N. Tripathi [a], V. Jindal [a], F. Shahedipour-Sandvik [a,*], S. Rajan [b], A. Vert [c]

[a] College of Nanoscale Science and Engineering, University at Albany, Albany, NY 12203, USA
[b] Electrical and Computer Engineering Department, Ohio State University, OH 43210, USA
[c] General Electric, Global Research Center, Niskayuna, NY 12309, USA

ARTICLE INFO

Article history:
Received 4 November 2009
Received in revised form 24 May 2010
Accepted 9 June 2010
Available online 8 July 2010
The review of this paper was arranged by Prof. E. Calleja

Keywords:
GaN
HEMT
MOCVD
Enhancement mode

ABSTRACT

A novel device design for enhancement mode operation of III-nitride high electron mobility transistor (HEMT) structure has been proposed and demonstrated. The proposed HEMT device structure consists of a multi-heterojunction (SiO_2/$Al_xGa_{1-x}N$/GaN/$Al_yGa_{1-y}N$) design in contrast to a single AlGaN/GaN heterojunction commonly used in conventional III-nitride HEMT designs. Normally OFF operation of the proposed HEMT design is expected to take place for thicker GaN and the top $Al_xGa_{1-x}N$ layers than previously allowed. The effects of design parameters on the value of the device turn ON voltage have been studied extensively using simulations. Various device structures have been developed based on the simulations results and epitaxially grown by MOCVD. *I–V* measurements support the effects of design parameters on the turn ON voltage predicted by the simulations and have confirmed the enhancement mode operation.

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have attracted a lot of attention for the purpose of development of high power and high frequency transistors. Spontaneous and piezoelectric polarization present in nitride devices grown in the *c*-crystallographic direction induce high density of two-dimensional electron gas (2DEG). Furthermore, high carrier saturation velocities and high breakdown voltage of the III-nitride material system allows development of the state of the art transistors with maximum oscillating frequencies as high as 230 GHz [1] and power of 250 W [2]. Conventional AlGaN/GaN HEMT device consists of a single heterojunction between a thin AlGaN layer (~30 nm) deposited on thick GaN template. Such HEMT devices operate in depletion mode (normally ON). Even though conventional AlGaN/GaN HEMTs have met ever increasing demands of high frequency and high power applications, development of III-nitride based HEMTs with enhancement mode (normally OFF) operation is still at its early stages, as it is clear from very small number of reports on such devices. Normally OFF devices offer reduced power consumption, reduced circuit complexity and safer operation. Few attempts have been made and reported in literature that utilizes modification of conventional depletion mode design to achieve enhancement mode operation [3–8].

In conventional single heterojunction AlGaN/GaN HEMT, difference in polarization between the two device layers induces fixed positive polarization charges at the AlGaN/GaN interface. These fixed positive charges induce a high density of 2DEG in the GaN layer at the AlGaN/GaN interface even at 0 V of applied bias.

AlGaN/GaN recessed MIS-gate HFET design reported by Oka et al. achieves high positive turn ON voltage but at the cost of using metal–insulator–GaN based gate structure [9]. Such structure compromises on the advantages of using high quality epitaxial AlGaN–GaN interface as the channel region. A comparative study performed by Sugiura et al. demonstrates that the carriers at insulator–GaN interface suffer from degradation in mobility by more than one order of magnitude as compared to carriers at AlGaN–GaN interface [10].

The dual heterojunction, back barrier $Al_xGa_{1-x}N$/GaN/$Al_yGa_{1-y}N$ HEMT design reported by Chu et al. operates in enhancement mode [11]. Turn ON voltage in this design is determined by the interaction between the polarization induced fixed charges at the bottom GaN/$Al_yGa_{1-y}N$ and top $Al_xGa_{1-x}N$/GaN interfaces. The normally OFF operation of this device design in contrast to normally ON operation of conventional AlGaN/GaN design is a direct consequence of the additional negative polarization sheet charges in the former design. Presence of the additional negative fixed charges at the bottom GaN/$Al_yGa_{1-y}N$ interface increases the local

* Corresponding author.
E-mail address: sshahedipour@uamail.albany.edu (F. Shahedipour-Sandvik).

0038-1101/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2010.06.008

potential energy of the electrons in the GaN layer resulting in the absence of 2DEG at 0 V of applied bias. Thin AlGaN top barrier layer (gate to channel distance of 5 nm) was required to achieve normally OFF operation at low positive (less than 0.5 V) turn ON voltages. Increase in thickness of either the GaN or the top AlGaN layer leads to accumulation of 2DEG at the top AlGaN/GaN interface due to reduced influence of the negative polarization charges on the top AlGaN/GaN interface. Due to the design requirements, development of such device structures involves multiple growth challenges including growth of high quality thick AlGaN layer with smooth surface used as a template for subsequent growth of the thin GaN and AlGaN layers. Further, exceptional uniformity in the thickness of the thin GaN and top AlGaN layers are required to achieve uniformity in turn ON voltage for various devices on the wafer. Such stringent requirement may not be met given the inherent, although small, growth nonuniformities in growth systems.

Here we report on a novel device design with an additional SiO_2/AlGaN interface that provides three significant advantages over the dual heterojunction design reported previously. Additional sheet of induced negative polarization fixed charges allows for implementation of a much thicker top AlGaN barrier layers, provides higher turn ON voltages as compared to the reported dual heterojunction design, and provides a limited control over the value of turn ON voltage.

2. Simulations

Energy band diagrams for the proposed designs were simulated using Sentaurus [12] device simulator that includes Ambacher et al. formulation of polarization charges at AlGaN/GaN interfaces [13]. All the III-nitride layers have been assumed to be fully relaxed in the simulations. Negative fixed charges at the $SiO_2/Al_xGa_{1-x}N$ interface have been assumed to be $4.5 \times 10^{12}\ cm^{-2}$ and $6.5 \times 10^{12}\ cm^{-2}$ for $x = 0.15$ and 0.30, respectively. Experimentally measured density of negative fixed charges at SiO_2/AlGaN interface has been reported to be of similar magnitude [14]. Design 1 (inset in Fig. 1) includes deposition of an additional layer of SiO_2 on top of the $Al_{0.15}Ga_{0.85}N/GaN/Al_{0.10}Ga_{0.90}N$ heterostructure. Barrier height of 4.0 eV between gate oxide and metal contact has been used in all simulations. As can be seen in the simulated energy band diagram for this device (Fig. 1), normally OFF operation is expected even with thicker GaN and top AlGaN layers. In this design, the additional SiO_2 layer deposited on top of the $Al_xGa_{1-x}N$ layer induces a fixed negative sheet charge [14], in addition to the other two polarization induced sheet charges observed in the previous design. The additional negative fixed charge at the $SiO_2/Al_xGa_{1-x}N$ interface raises the potential energy of the $Al_xGa_{1-x}N$/GaN interface resulting in the normally OFF operation. Such device design is preferred as it provides greater tolerance with respect to the bottom $Al_yGa_{1-y}N$ surface roughness and is less sensitive to the GaN layer thickness.

Device characteristics such as turn ON voltage and I_{ON}/I_{OFF} ratio for such device design are governed by the interaction of the polarization induced charges at the three heterojunctions. Simulations were performed to deconvolute effects of the $Al_{0.15}Ga_{0.85}N$ and GaN thicknesses on device characteristics. Designs with 5, 15, 25, 35, 45 and 55 nm of GaN thicknesses with each of 5, 15, 25, 35, 45 and 55 nm of top $Al_{0.15}Ga_{0.85}N$ thicknesses were simulated. Two different parameters were monitored, (a) electron (e^-) density at the $Al_{0.15}Ga_{0.85}N$ and GaN interface at 0 V of applied bias; and (b) the lowest bias to the top SiO_2 that is required to induce an electron density of greater than $1 \times 10^{19}\ cm^{-3}$ in the channel, turning the device ON.

Fig. 2 summarizes the calculated electron density at the $Al_{0.15}Ga_{0.85}N$/GaN interface for all the combinations of GaN and $Al_{0.15}Ga_{0.85}N$ thicknesses mentioned above. Very low electron density at 0 V applied bias is required to minimize the OFF current. As expected, electron density reduces with reduction in the thickness of the GaN and $Al_{0.15}Ga_{0.85}N$ layers. Simulations suggest that thickness of the top $Al_{0.15}Ga_{0.85}N$ plays a more important role in controlling the 0 V electron density, with a smaller but considerable effect from the GaN thickness. This behavior can be qualitatively attributed to the higher polarization induced negative charges at the $SiO_2/Al_{0.15}Ga_{0.85}N$ interface compared to the negative charges induced at the $GaN/Al_{0.10}Ga_{0.90}N$ interface.

Table 1 tabulates the lowest turn ON (TO) voltage required to induce an electron density greater than $1 \times 10^{19}\ cm^{-3}$ in the channel. Devices with 45 nm/55 nm and 55 nm/55 nm thickness values for $Al_{0.15}Ga_{0.85}N$/GaN layers show $>1 \times 10^{19}\ cm^{-3}$ electron density with 0 V of applied bias. Once again, higher dependence of the TO voltage on the $Al_{0.15}Ga_{0.85}N$ thickness is observed. One should note that lower TO voltages can be achieved for thicker layers but higher electron density exists at $Al_{0.15}Ga_{0.85}N$/GaN interface for such design at 0 V that would lead to higher OFF current.

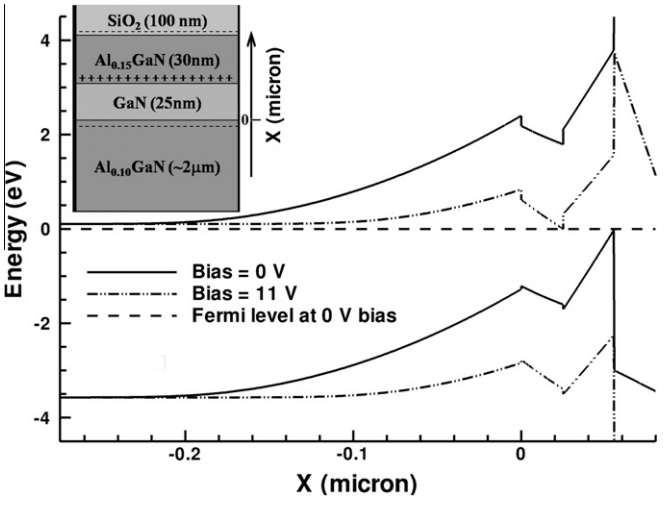

Fig. 1. Simulated energy band diagram of a modified back barrier HEMT structure. *Y*-axis represents the energy and *X*-axis represents the distance along the device structure where $GaN/Al_{0.10}Ga_{0.90}N$ heterojunction is always kept at $X = 0$. Device design is shown in the inset.

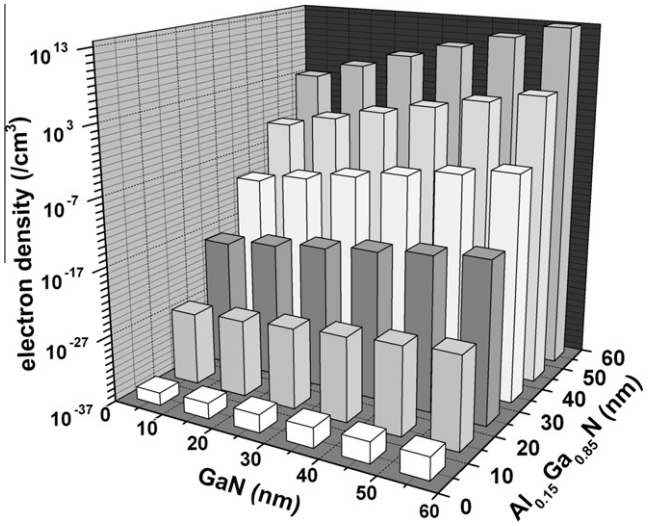

Fig. 2. 3D plot showing variation of electron density at GaN and $Al_{0.15}Ga_{0.85}N$ interface for different thicknesses of the GaN and $Al_{0.15}Ga_{0.85}N$ layers, as calculated by simulations.

Table 1
Lowest simulated voltage required to induce electron density greater than 1×10^{19}/cm^3 in the GaN channel for devices with different GaN and $Al_{0.15}Ga_{0.85}N$ thicknesses. Voltage values are given in units of volts.

AlGaN (nm)	GaN 5 nm	15 nm	25 nm	35 nm	45 nm	55 nm
5	17.0	16.5	16.0	15.5	15.0	14.5
15	16.5	16.0	15.5	15.0	14.5	14.0
25	16.5	15.5	15.0	14.5	14.0	13.5
35	16.0	15.0	14.5	14.0	13.5	13.0
45	15.5	14.5	14.0	13.5	12.5	12.5
55	15.0	14.0	13.5	12.5	12.0	12.0

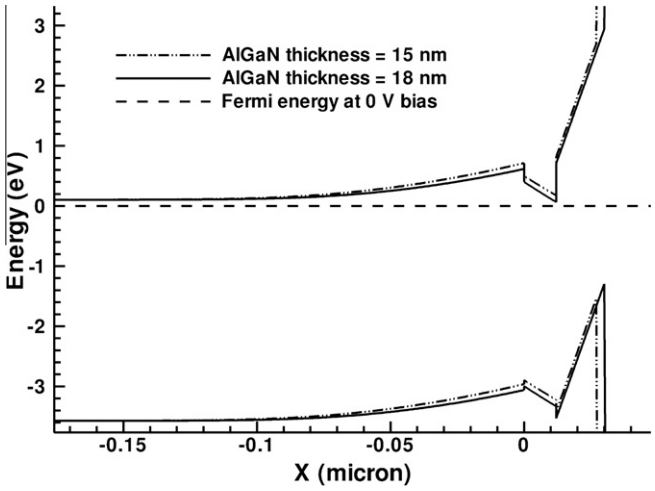

Fig. 3. Simulated energy band diagrams for back barrier device structures with 15 nm and 18 nm of top $Al_{0.30}Ga_{0.70}N$ thickness. Thickness of GaN layer and $Al_{0.10}Ga_{0.90}N$ layer used for both structures were 12 nm and 1 μm, respectively. A normally OFF operation is predicted for design given with 15 nm of top $Al_{0.30}Ga_{0.70}N$.

Effect of the composition of the top $Al_xGa_{1-x}N$ layer on turn-ON voltage was studied by increasing the composition of the top $Al_xGa_{1-x}N$ layer from 15% to 30% in Design 1. Simulation results suggest that such change in the $Al_xGa_{1-x}N$ composition will result in normally ON operation for this design. This can be attributed to increased density of the polarization induced positive charges at the $Al_{0.3}Ga_{0.7}N$/GaN interface. Increased positive charge density at this interface lowers the potential energy at the interface resulting in accumulation of 2DEG in the GaN layer at 0 V of applied bias. With increased composition of aluminum in the top AlGaN, normally OFF operation could be achieved by reducing thickness of the GaN and $Al_{0.3}Ga_{0.7}N$ layers. Such reduction enhances the influence of the top and the bottom negative sheet charges in raising potential energy at $Al_{0.3}Ga_{0.7}N$/GaN interface to above the device Fermi level. Fig. 3 shows simulation results for this device with GaN thickness of 12 nm, and $Al_{0.3}Ga_{0.7}N$ thickness of 15 nm (Device 2) and 18 nm (Device 3) respectively. Simulation results suggest that the design with thinner $Al_{0.3}Ga_{0.7}N$ layer has about two orders of magnitude lower electron density (2.8×10^{15} cm^{-3}) than the device with 18 nm of $Al_{0.3}Ga_{0.7}N$ layer (2.0×10^{17} cm^{-3} of electrons in the channel region).

3. Experimental results and discussion

Device structure based on the Design 1 was grown by metalorganic chemical vapor deposition (MOCVD) in a Veeco D180 rotating disk reactor using Trimethylaluminum (TMAl), Trimethylgallium (TMGa), Ammonia (NH3) and purified Hydrogen as a carrier gas. Two micron thick $Al_{0.10}Ga_{0.90}N$ was grown on a Sapphire substrate using thin, low temperature AlN buffer. Exhaustive optimization of growth parameters including AlN buffer thickness, growth pressure and V/III ratio was performed to obtain smooth $Al_{0.10}Ga_{0.90}N$ surface with RMS roughness of 0.85 nm for a $2\ \mu m \times 2\ \mu m$ surface (not shown here). GaN (25 nm) and $Al_{0.15}Ga_{0.85}N$ (30 nm) layers were deposited on the $Al_{0.10}Ga_{0.90}N$ template. Surface morphology of the complete device structure (top $Al_{0.15}Ga_{0.85}N$ layer) shows smooth surface with visible atomic steps. Depth resolved Auger electron spectroscopy (AES) was done to calculate approximate values of the composition and thickness of various layers in the structure. AES results for this structure suggest thickness values of 30 nm and 40 nm for GaN and top AlGaN layers; and Al incorporation of 10% and 15% in the bottom and top AlGaN layers, respectively. Ti (15 nm)/Al (60 nm)/Mo (40 nm)/Au (80 nm) metal stack source and drain contacts were deposited on $Al_{0.15}Ga_{0.85}N$ using e-beam evaporation. The deposited metal stack was annealed in the AG Heatpulse rapid thermal processor with nitrogen ambient for 60 s at 850 °C. Low-pressure chemical vapor deposition (LPCVD) was used to deposit 100 nm of SiO_2 on the $Al_{0.15}Ga_{0.85}N$ layer at 500 °C. Ni/Au metal stack gate contacts were then deposited on top of SiO_2 layer. Drain current (Fig. 4a) as a function of gate voltage, measured using a Keithley 4200 parameter analyzer, shows threshold voltage of +1.6 V for

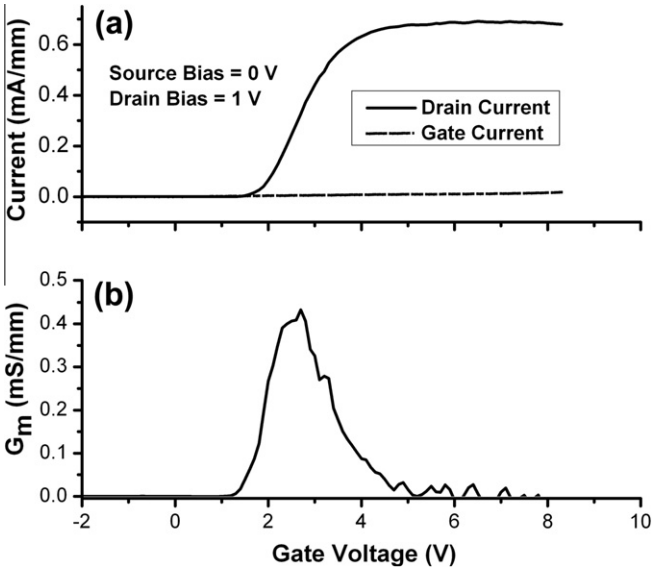

Fig. 4. (a) Drain current–gate voltage characteristic for Device 1 confirming positive turn ON voltage for this design; (b) transconductance (G_m) as a function of gate bias.

Table 2
List of experimentally tested device dimensions and observed turn ON voltages.

Device #	GaN thickness (nm)	$Al_xGa_{1-x}N$ composition/ thickness (nm)	SiO_2 thickness (nm)	Threshold (V)
1	25	0.15/30	100	+1.6
2	12	0.30/15	100	+0.7
3	12	0.30/18	100	−11.0
	Source–gate distance (μm)	Gate length (μm)	Gate–drain distance (μm)	Gate width (μm)
1	2	7	15	100
2	5	9	20	50
3	2	4	6	100

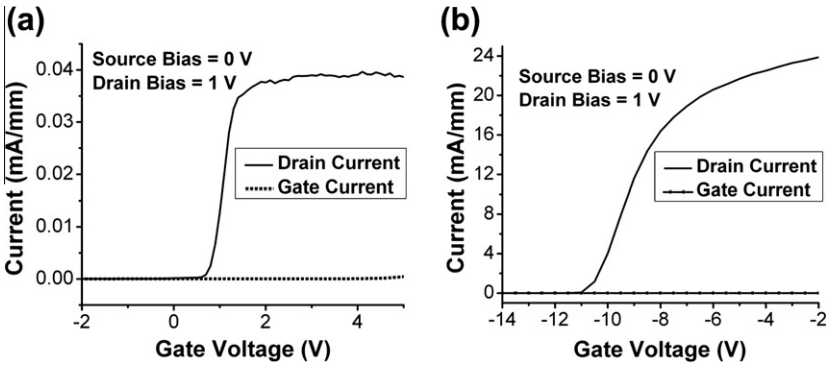

Fig. 5. Drain current–gate voltage characteristic for (a) Device 2; and (b) Device 3 confirming simulation results given in Fig. 3.

Device 1, confirming enhancement mode operation, as predicted by simulations. Fig. 4b shows variation on transconductance (G_m) as a function of gate bias with peak value of 0.43 mS/mm at gate bias of 2.7 V. This result emphasizes that proposed device design has the potential to achieve higher turn ON voltages. (see Table 2).

Device 2 and Device 3 designs were then grown using the same growth method and growth conditions. 12 nm GaN was deposited on $Al_{0.10}Ga_{0.90}N$ template followed by deposition of 30 nm of $Al_{0.30}Ga_{0.70}N$. After deposition of source and drain metal contacts, recessed gates were made with etch depth of 15 nm (Device 2) and 18 nm (Device 3). Gate metal contacts were deposited after deposition of 100 nm of SiO_2 in the gate region. Drain current as a function of gate voltage was measured and are shown in Fig. 5a and b. The device with thicker $Al_{0.30}Ga_{0.70}N$ barrier shows negative turn ON voltage where as the device with thinner $Al_{0.30}Ga_{0.70}N$ shows positive turn ON voltage. These results demonstrate how thickness and composition of the different device layers can be modified to control the turn ON voltage of the proposed normally OFF device. This also confirms that the turn ON voltage has strong dependence on the thickness of the nitride layers.

4. Summary

A novel SiO_2/AlGaN/GaN/AlGaN back barrier HEMT design has been proposed and developed that demonstrates the enhancement mode operation of III-nitride based HEMT. Exhaustive growth and simulations were performed to understand the effect of various design parameters, including thickness and composition of GaN and AlGaN layers, on the device turn-on characteristics. Three types of devices with different design parameters are developed and characterized to establish dependence of threshold voltage on the device design parameters. Analytical rationale for the observed variation of threshold voltage in different designs has been provided in terms of the density of the polarization induced charges at various interfaces.

Acknowledgement

Funding for this work was provided by General Electric Global Research Center in Niskayuna, NY.

References

[1] Palacios T, Chakraborty A, Heikman S, Keller S, DenBaars SP, Mishra UK. AlGaN/GaN high electron mobility transistors with InGaN back-barriers. IEEE Electron Dev Lett 2006;27:13–5.
[2] Kikkaw T, Joshin K. High power GaN-HEMT for wireless base station applications. IEICE Trans Electron 2006;E89-C:608–15.
[3] Endoh A, Yamashita Y, Ikeda K, Higashiwaki M, Hikosata K, Matsui T, et al. Non-recessed-gate enhancement-mode AlGaN/GaN high electron mobility transistors with high RF performance. Jpn J Appl Phys 2004;43:2255–8.
[4] Palacios T, Suh C-S, Chakraborty A, Keller S, DenBaars SP, Mishra UK. High-performance E-mode AlGaN/GaN HEMTs. IEEE Electron Dev Lett 2006;27:428–30.
[5] Khan MA, Chen Q, Sun CJ, Yang JW, Blasingame M, Shur MS, et al. Enhancement and depletion mode GaN/AlGaN heterostructure field effect transistors. Appl Phys Lett 1996;68:514–6.
[6] Lanford WB, Tanaka T, Otoki Y, Adesida I. Recessed-gate enhancement-mode GaN HEMT with high threshold voltage. Electron Lett 2005;41:449–50.
[7] Cai Y, Zhou Y, Chen KJ, Lau KM. High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment. IEEE Electron Dev Lett 2005;26:435–7.
[8] Micovic M, Tsen T, Hu M, Hashimoto P, Willadsen PJ, Milosavljevic I, et al. GaN enhancement/depletion-mode FET logic for mixed signal applications. Electron Lett 2005;41:1081–3.
[9] Oka T, Nozawa T. AlGaN/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications. IEEE Electron Dev Lett 2008;29:668–70.
[10] Sugiura S, Hayashi Y, Kishimoto S, Mizutani T, Kuroda M, Ueda T, et al. Fabrication of normally-off mode GaN and AlGaN/GaN MOSFETs with HfO_2 gate insulator. Solid-State Electron 2010;54:79–83.
[11] Chu R, Chen Z, DenBaars SP, Mishra UK. *V*-gate GaN HEMTs with engineered buffer for normally off operation. IEEE Electron Dev Lett 2008;29:1184–6.
[12] http://www.synopsys.com/Tools/TCAD/DeviceSimulation/Pages/SentaurusDevice.aspx.
[13] Ambacher O, Smart J, Shealy JR, Weimann NG, Chu K, Murphy M. Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructure. J Appl Phys 1999;85:3222–33.
[14] Vert A, Rajan S. Properties of oxide deposited on c-plane AlGaN/GaN heterostructure. Electron Lett 2008;44:773–4.