p-Type SiGe Transistors with Low Gate Leakage Using SiN Gate Dielectric

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***Abstract*—Using high-quality jet-vapor-deposited (JVD) SiN as gate dielectric, p-type SiGe transistors are fabricated on SiGe heterostructures grown by ultra-high-vacuum chemical vapor deposition (UHVCVD). For an 0.25-μm gate-length device, the gate leakage current is as small as 2.4 nA/mm at $V_{ds} = -1.0$ V and $V_{gs} = 0.4$ V. A maximum extrinsic transconductance of 167 mS/mm is measured. A unity current gain cutoff frequency of 27 GHz and a maximum oscillation frequency of 45 GHz are obtained.**

I. Introduction

THE application of SiGe bandgap engineering concept to silicon technology has made possible the fabrication of devices that were previously only feasible in other material systems. Si/SiGe heterobipolar transistors with demonstrated unity current gain cutoff frequencies (f_T) and maximum oscillation frequencies $(f_{\rm MAX})$ well beyond 100 GHz have promoted Si-based technologies into an area that has, so far, been an exclusive domain of III–V devices. Si/SiGe modulation-doped field effect transistors (MODFET's) have also demonstrated excellent characteristics. For p-SiGe MODFET's, an f_T of 70 GHz and an $f_{\rm MAX}$ of 85 GHz have been reported [1], [2]. For n-type SiGe MODFET's, an f_T of 62 GHz and an $f_{\rm MAX}$ of 92 GHz have been achieved [3]–[5]. However, relatively high gate leakage current hinders the usefulness of these devices [4], [6]. The insertion of an oxide insulating layer between the SiGe channel and the gate could surmount the limitation. This could make possible the realization of high-speed metal–oxide–semiconductor field effect transistor (MOSFET)-type devices which take advantage of both the superior electron and hole transport properties in strained Si/SiGe layers. So far, several groups have reported results of p- and n-type MOSFET's in which strained SiGe or Si layers were used as channels [7]–[14]. A maximum dc extrinsic transconductance (g_m) for an 0.25-μm channel length SiGe p-MOSFET of 167 mS/mm was achieved using a buried SiGe as channel, which was separated from a gate oxide dielectric by a silicon cap layer [7]. To our knowledge, the highest reported f_T for a p-MOSFET with a modulation-doped SiGe heterostructure (MOS-MODFET) is 23 GHz [10]. Conventional thermal oxide is not an optimal candidate for gate dielectrics in SiGe MOSFET's because its high processing temperature may cause the relaxation of strained SiGe layers and segregation of Ge atoms, which would significantly degrade the gate oxide quality. Jet-vapor-deposited (JVD) oxide, deposited directly on Si at room temperature, has demonstrated excellent electronic properties [15]. To further suppress the tunneling current, high dielectric constant material, e.g., SiN_x, is an attractive candidate in place of ultrathin oxide. Ma [15] and Tseng *et al*. [16] have demonstrated that JVD nitride with 3 nm equivalent-oxide-thickness (EOT) has 100 times lower leakage than thermal oxide with the same EOT on bulk Si CMOS, and the interface stability of JVD nitride compares favorably with thermal oxide. In this letter, for the first time, we report our results on the fabrication and characterization of p-type SiGe MOS-MODFET's with ultrathin JVD nitride gate dielectric.

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II. Device Structrue and Rpocessing

The heterostructure was grown by ultra-high-vacuum chemical vapor deposition (UHVCVD) on an n^- Si substrate. The layer sequence starts with a linearly step-graded $Si_{(1-x)}Ge_x$ buffer layer relaxed to the lattice constant of $Si_{0.7}Ge_{0.3}$. A 1-μm thick $Si_{0.7}Ge_{0.3}$ buffer layer is followed by the modulation-doped structure consisting of, from bottom to top, a 4-nm B-doped $Si_{0.7}Ge_{0.3}$ supply layer at a doping density of 2×10^{18} cm^{-3}, a 3-nm undoped $Si_{0.7}Ge_{0.3}$ spacer, and a 4.5-nm thick $Si_{(1-x)}Ge_x$ channel graded from 0.8 to 0.7, and a 10-nm $Si_{0.7}Ge_{0.3}$ cap layer. Compared to conventional MODFET's [1], [17], the thinner cap layer was used to guarantee that the high mobility carriers in the SiGe quantum well can be well modulated while the buried channel provides benefits such as suppression of hot-carrier injection into the gate dielectric and reduced carrier surface scattering which tend to enhance device performance and reliability. The layer exhibited a two-dimensional hole-gas mobility of 930 cm^2/Vs and a hole sheet density of 2.6×10^{12} cm^{-2} at room temperature.

The device processing started with the deposition of SiN using the JVD method. The details and optimization of the JVD process are presented elsewhere [15]. To densify the film, the sample received a rapid thermal annealing treatment at 500 °C for 30 s.. The temperature was kept low to prevent Ge segregation. The physical thickness of the nitride film was

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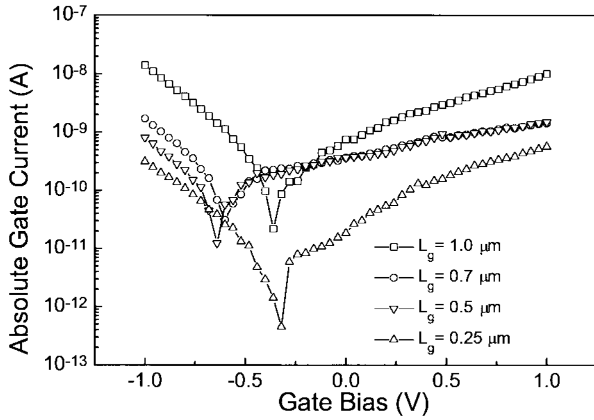


Fig. 1. Gate current as a function of gate voltage for four transistors with $L_g = 0.25, 0.5, 0.7, 1.0\ \mu$m ($W_g = 50\ \mu$m) at drain bias $V_{ds} = -1.025$ V.

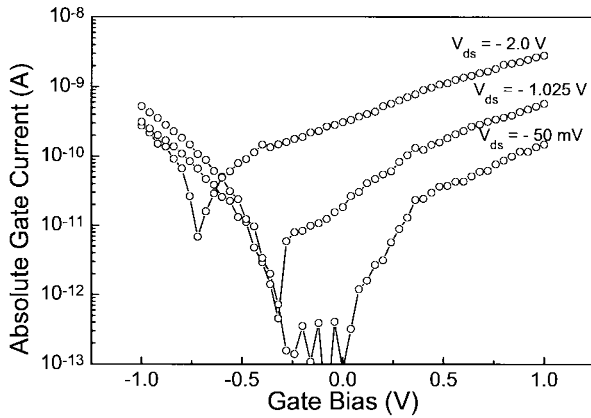
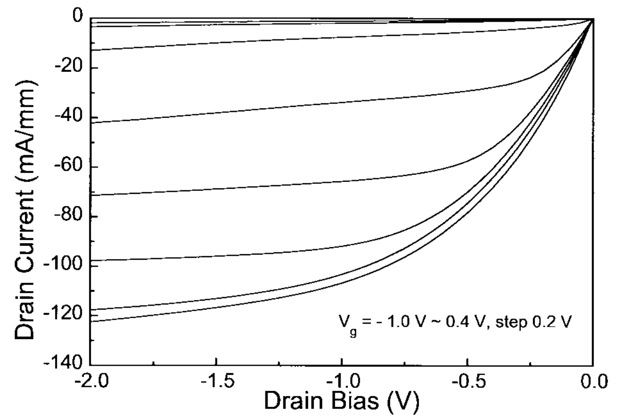
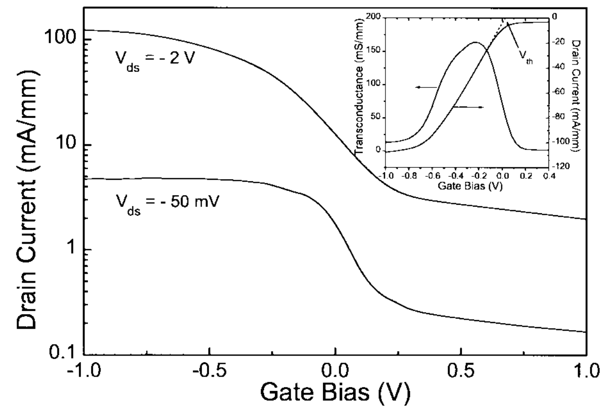


Fig. 2. Gate current as a function of gate bias for a 0.25-μm gate-length device with 50-μm gate-width at drain biases of -2 V, -1.025 V, and 50 mV.



(a)



(b)

Fig. 3. (a) I_d–V_d characteristics, gate bias swept from -1.0 V to 0.4 V in 0.2-V steps, and (b) subthreshold drain current versus gate voltage for a device with 0.25-μm gate-length and 50-μm gate-width. The inset shows the extrinsic transconductance and drain current as a function of gate voltage at drain bias $V_{ds} = -0.8$ V.

about 5 nm, which corresponded to an EOT of 3 nm. Mesa-isolation by reactive ion etching in CF_4 plasma was carried out to define the device active area. The mesa height was 240 nm. Then, the sample was passivated using 280-nm thick SiO_2. Ohmic metallization consisting of 30-nm Pt was evaporated and lifted off after the silicon nitride in the ohmic area was etched off using buffered HF. A contact resistance of 0.2–0.3 Ω-mm was obtained after the sample was sintered in a nitrogen ambient at 350 °C for 5 min. Mushroom Ti/Al/Pd gates with various gate lengths (0.25, 0.5, 0.7, and 1 μm) were patterned with a trilayer resist system using electron beam lithography. The Pd was used for preventing the oxidation of aluminum. The source-drain distance is 2 μm for all devices except those with 1-μm gate length in which the source-drain distance is 3 μm.

III. Results and Discussion

Fig. 1 shows the gate leakage current of devices with 50-μm gate width and different gate lengths at a drain bias of -1.025 V. As expected, the gate current scales with gate length. But at reverse gate bias, the 0.7-μm device has only slightly higher gate current than the 0.5-μm device. This is probably due to slight differences in the gate-source spacings. At $V_{gs} = -1.0$ V, the gate current density is 2.4, 3.1, 4.8, and 28.0 mA/cm^2 for $L_g = 0.25$, 0.5, 0.7, and 1.0 μm, respectively, which are much smaller than the maximum gate leakage requirement of 1 A/cm^2 imposed by the limitation of chip standby power. This shows the high quality of the JVD silicon nitride gate dielectric layer. On the other hand, no hard breakdown is observed for JVD nitride MOS capacitors under a gate bias of 7 V, which safely fulfills the requirement of the gate operation range of our devices. Fig. 2 shows gate current as a function of V_{gs} at different drain biases for a typical 0.25-μm gate-length device with a gate width of 50 μm. At a drain bias V_{ds} of -50 mV, the gate leakage current is -5.2×10^{-10} A and 1.4×10^{-10} A at gate biases, V_{gs}, of -1 V and 1 V, respectively. Compared to a conventional MODFET with a Schottky gate, this gate current is three orders of magnitude smaller than that at the same reverse bias and seven orders of magnitude smaller than that at the same forward bias [17]. Fig. 3(a) shows the dc characteristics of a typical device with 0.25-μm gate-length. The device has good pinchoff with an off-state current less than 1 mA/mm for $V_{ds} < 1$ V. At $V_{ds} = -1.0$ V and $V_{gs} = 0.4$ V, the off-state gate leakage current is only 2.4 nA/mm. So, its contribution to the subthreshold current is negligible. Therefore, the subthreshold current, shown in Fig. 3(b), is due to buffer leakage below the channel. Further reduction of drain

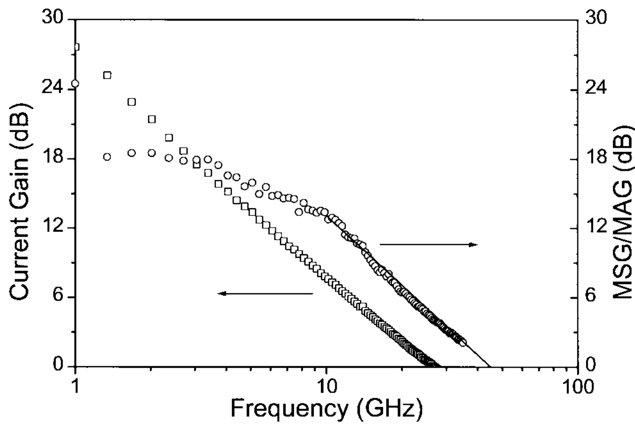


Fig. 4. Measured current gain ($|h21|$), maximum stable gain (MSG) and maximum available gain (MAG) versus frequency for a 0.25-μm gate-length device with 100-μm gate-width biased at $V_{\rm ds} = -0.8$ V, and $V_{\rm gs} = -0.25$ V.

subthreshold current can be expected by optimization of layer structure design and growth. The g_m and drain current as a function of gate bias at a drain bias $V_{\rm ds}$ of -0.8 V are shown in the inset of Fig. 3(b). A maximum g_m of 167 mS/mm was measured at a gate bias of -0.24 V. By defining the threshold voltage ($V_{\rm th}$) as the gate bias intercept of the extrapolation of $I_{\rm ds}$ at the point of maximum g_m, we estimate that the threshold voltage $V_{\rm th}$ is 0.023 V.

For RF characteristics, the S-parameters of the devices were measured in the range of 1–35 GHz using an HP8510B network analyzer. The current gain $|h21|$, the maximum stable gain (MSG) and the maximum available gain (MAG) are plotted against frequency in Fig. 4. An $f_T = 27$ GHz and an $f_{\rm MAX} = 45$ GHz were obtained at a drain bias of -0.8 V and a gate bias of -0.25 V. To our knowledge, these are the highest data reported so far for any SiGe heterojunction MOSFET's. All these attractive characteristics are attributed to the quality of layer structure and growth, high-quality gate dielectric layer deposition, and an optimized fabrication process.

IV. Conclusion

In this letter, we have reported the characteristics of p-type SiGe MOS transistors with JVD SiN gate dielectrics fabricated on UHV-CVD-grown SiGe heterostructures. The use of a 5-nm thick SiN film, which is equivalent to 3-nm thick oxide, demonstrated significantly low gate leakage current. For devices with 0.25-μm gate length, a maximum g_m of 167 mS/mm was obtained. An f_T of 27 GHz and an $f_{\rm MAX}$ of 45 GHz have been achieved. These dc and RF characteristics are comparable with state-of-art SiGe MODFET's but with much lower gate leakage current. The drain subthreshold current can be reduced by further optimization of buffer-layer growth techniques.

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